A NEW MINIMIZATION TECHNIQUE OF THE ERROR IN SHORT-CHANNEL MOSFET CIRCUITS RESULTING FROM CARRIER MOBILITY REDUCTION

BY

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This thesis is dedicated to

my parents, my brothers, my sisters

my wife, and my sons Ali and Ahmed,

for their love, endless support and encouragement

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First and foremost, I thank ALLAH for all the blessings and wonderful opportunities. He has bestowed upon me in my journey through life. It is only by his grace that I have had the ability and strength to overcome life's challenges.

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LIST OF ABBREVIATIONS

***MOSFET**: Metal Oxide Semiconductor Field Effect Transistor*

***MOS:** Metal Oxide Semiconductor*

***CMOS:** Complementary MOS*

***PMOS**: P-channel MOSFET*

***NMOS**: N-channel MOSFET*

***MTL**: MOSFET Translinear Loop*

***VLSI:** Very Large Scale Integration*

***AC:** Alternating Current*

***DC:** Direct Current*

***V:** Voltage*

***I:** Current*

***I_D:** Drain Current*

***R:** Resistor*

***M:** Transistor*

***λ:** Channel Length Modulation Factor*

***θ:** Fitting Parameter*

***k'_n:** Process Transconductance Parameter*

***W:** Channel Width*

***L:** Channel Length*

β: *Transconductance Parameter=(k'_n*W/L)*

V_{GS}: *Gate to Source Voltage*

V_{DS}: *Drain to Source Voltage*

V_{SB}: *Source to Body Voltage*

V_{TH}: *Threshold Voltage*

V_{THO}: *Zero-bias Threshold Voltage*

V_C: *Controllable Voltage*

V'_A: *Entirely Process Technology*

ϕ_b *: Bulk Potential*

Δ***L:*** *Mismatch term of L*

Δ***V_{TH}:*** *Mismatch term of V_{TH}*

μ_0: *Low Field Mobility*

cw: *Clockwise*

ccw: *Counter-clockwise*

T: *Absolute Temperature*

ABSTRACT

FULL NAME : IBRAHIM ALI ABU-BAKR AS-SABBAN

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As the transistor is scaled down, second order effects should be included in the analysis. Consequently, the square law drain current equation is not valid anymore and hence a way to compensate for the errors due to these effects should be considered. The main effects that can be compensated for are the channel length modulation, body effect and the carrier mobility reduction. For example, at large gate-source voltage, the high electric field developed between the gate and the channel confines the charge carrier to a narrower region below the oxide-silicon interface, leading to more carrier scattering and hence lower mobility. In this work, a new minimization technique to cancel the error in short-channel MOSFET circuits resulting from carrier mobility reduction is proposed. The proposed technique is used in redesigning some analog computational circuits like square-rooting circuit, squaring circuit and multiplying circuit based on MOS translinear loop principle operating in strong inversion. The proposed circuits are simulated using T-spice in 0.18µm CMOS technology.

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ملخص الرسالة

الاسم الكامل: إبراهيم علي أبوبكر الصبان

عنوان الرسالة: طريقة جديدة لتقليل الخطأ الناجم عن تأثير حركة الإلكترونات عبر القناة في الدوائر الكهربائية والتى تستخدم ترانزستور قصير القناة من نوع MOSFET.

التخصص: هندسة كهربائية

تاريخ الدرجة العلمية: ديسمبر 2013

من المعلوم أنه كلما قل حجم الترانزيستور فإن العوامل الثانوية المؤثره في أدائه تزداد بشكل كبير وبالتالى فإن هذه العوامل تكون مهمة جدا ويجب اخذها بعين الاعتبار في تصميم الدوائر الإلكترونية. وأهم العوامل المؤثره هي تأثير طول القناة و حركة الإلكترونات في القناة.فمثلا عند زيادة الجهد بين البوابة والمصدر للترانزيستور فإن المجال المغناطيسي بين البوابة والقناة يزداد بشكل كبير الامر الذي يؤدي الى الحد من تنقل الشحنات الكهربائية أسفل البوابة وبالتالي يزداد تشتت اللإلكترونات وهذا يحد من حركتها عبر القناة وهذ مايعرف بإسم (Carrier Mobility Reduction). هذا البحث يقدم طريقة جديده لتقليل الخطأ الناجم عن تأثير حركة الإلكترونات عبر القناة في الدوائر الكهربائية والتى تستخدم ترانزستور قصير القناة من نوع MOSFET. هذه الطريقة تم تطبيقها على دوائر تماثليه والتي شملت كل من دائرة الجذر التربيعي ودائرة التربيع ودائرة الضرب. تم تنفيذ جميع هذه الدوائر بأستخدام طريقة الحلقة أو مايعرف بإسم (Translinear Loop). تم محاكاة هذه الدوائر بإستخدام أحد البرامج المعتمدة من الصناعة Tanner T-Spice والذي أستخدم فيه نقنية ال CMOS 0.18µm.

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CHAPTER 1

INTRODUCTION

In order to realize higher-speed and higher packing density CMOS circuits, the dimensions of MOSFET transistors have continued to shrink according to the scaling law proposed in [1]. However, the low-voltage and low-power for submicron VLSI applications have become rather significant as a result of extremely large integration. Consequently, scaling of MOS dimensions is important in order to achieve higher-performance and higher-functional VLSI's. The gradual channel approximation used for long-channel MOSFET to develop the square-law V-I characteristics of the MOSFET is not suitable for modern short-channel devices.

It is well known that, as the channel length is reduced, the so-called short-channel effects arise. However, the short-channel effects are often attributed to the limitation imposed on electron drift characteristics in the channel and the modification of the threshold voltage. In particular, the short-channel effects can be physically classified by the so-called drain induced barrier lowering, surface scattering, velocity saturation, impact ionization and hot electrons. When the transistor size scaled down to deep nanometres, the traditional square-law characteristic and models cannot be used. Second order effects play an import role in short-channel MOSFET and cannot be ignored, otherwise the accuracy of the design will be degraded very much. More details about the second order effects are given below.

1.1 Short-channel MOSFETs and Second Order Effects

As circuits are designed using short-channel MOS transistors, second order effects become more important and require modifications to the MOS models or a way to compensate for the errors due to these effects. The main effects that can be compensated for are the channel length modulation, body effect and the carrier mobility reduction.

1.1.1 Channel- Length Modulation

The drain current equation including the channel length modulation only is given by:

$$I_D = \frac{\beta}{2}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \qquad (1.1)$$

Where $\beta = \mu_n C_{ox} \frac{W}{L}$ is the transconductance parameter, V_{GS} is the gate-source voltage, V_{TH} is the threshold voltage, V_{DS} is the drain to source voltage, and λ is the channel length modulation factor given by:

$$\lambda = \frac{1}{V'_A L} \qquad (1.2)$$

where V'_A is the value of entirely process-technology [2], L is channel length.

Channel length modulation is considered one of several short-channel effects in MOSFETs. It is well known that the channel length modulation factor (λ) increases as the channel length decrease as shown in table (1.1) [2].

Table 1.1 Channel length modulation factor for nMOS and pMOS in various technologies

CMOS Technology	λ nMOS	λ pMOS
0.8µm	$0.04v^{-1}$	$0.05v^{-1}$
0.5µm	$0.05v^{-1}$	$0.1v^{-1}$
0.18µm	$0.2v^{-1}$	$0.166v^{-1}$

1.1.2 Body Effect

In MOS transistor, the body effect occurs when the source terminal is not connected to the substrate or body terminal which is usually connected to the most negative power supply in an NMOS transistor and to the most positive in a PMOS transistor. The resulting reverse-bias voltage between the source and the body (V_{SB}) in an NMOS circuit will have an effect on the drain current of the MOS transistor [2].

Body effect is related to threshold voltage by the following equation:

$$V_{TH} = V_{THO} + \gamma\left(\sqrt{(2\phi_b + |V_{SB}|)} - \sqrt{2\phi_b}\right) \qquad (1.3)$$

Where V_{TH} is the threshold voltage, V_{THO} is the zero-bias threshold voltage, γ is the body-effect coefficient, and ϕ_b is the bulk potential. It is clear from equation (1.3) that the threshold voltage V_{TH} increases as the source-substrate voltage (V_{SB}) increases.

1.1.3 Temperature Effect

The drain current of the MOS transistor is temperature sensitive, due to the sensitivity of the threshold voltage V_{TH} and transconductance parameter β to temperature variation,

with reference to equation (1.1) as temperature increases, the magnitude of V_{TH} and β decrease. The decrease in V_{TH} causes the drain current to increase. At the same time, a decrease in β causes the drain current to decrease. However, at small V_{GS}, V_{TH} dominates and the drain current increases with increasing temperature. At higher V_{GS}, β dominates and the drain current decreases with increasing temperature. Figures (1.1) and (1.2) show how the drain current variation with temperature in a long-channel and short-channel CMOS technology respectively [3].

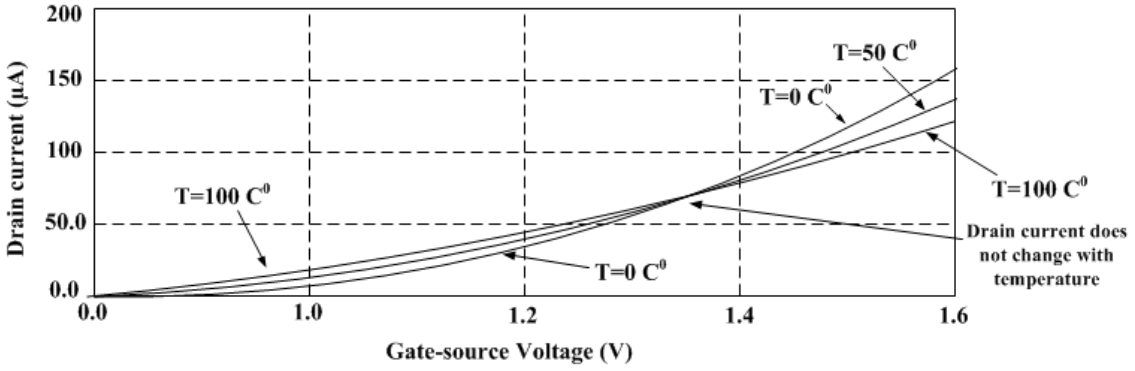

Figure 1.1 Long-channel drain current change with temperature [3]

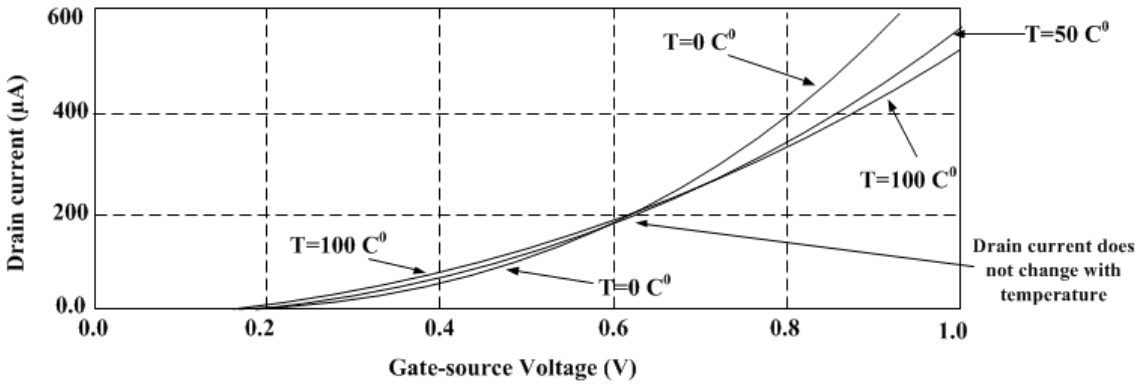

Figure 1.2 Short-channel drain current change with temperature [3]

1.1.4 Carrier Mobility Reduction

The gradual channel approximation used earlier to develop the square-law current-voltage characteristics of the MOSFET is not suitable for modern short-channel devices. The electric field under the gate oxide can no longer be treated in a single dimension. In addition, the velocity of the carriers drifting between the channel and the drain of the MOSFET can saturate and an effect called carrier velocity saturation (V_{sat}). The average drift velocity (v) of an electron plotted against electric field (E) is shown in Figure (1.3). When the electric field reaches a critical value (E_{cril}) the velocity saturates at V_{sat} that is the velocity cease to increase with increasing electric field. The ratio of electron drift velocity to applied electric field is the electron mobility [3] as the following equation;

$$\mu = \frac{v}{E} \tag{1.4}$$

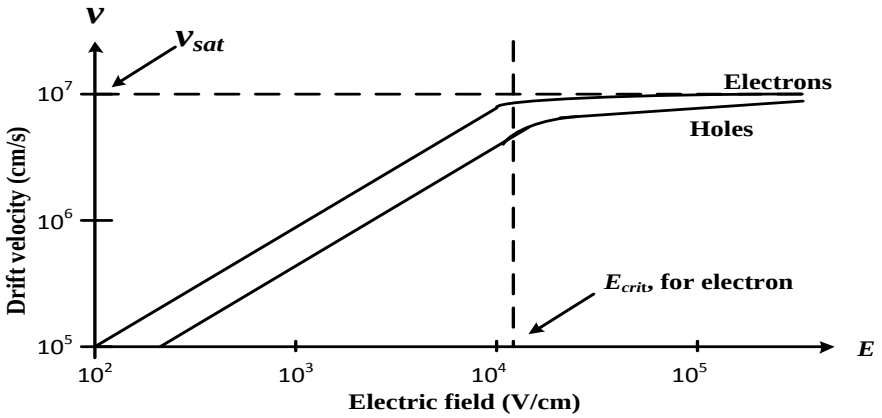

Figure 1.3 Drift velocity plotted against electric field [3]

With reference to Figure (1.3), above the E_{cril}, the mobility starts to decrease, whereas below E_{cril}, the mobility is essentially constant.

However, at large gate-source voltage, the high electric field developed between the gate and the channel confines the charge carrier to a narrower region below the oxide-silicon interface, leading to more carrier scattering and hence lower mobility. Since scaling has substantially deviated from the constant-field scenario, small-geometry devices experience significant mobility degradation. An empirical equation modelling mobility reduction is given by;

$$\mu_{eff} = \frac{\mu_0}{1+\theta(V_{GS}-V_{TH})} \tag{1.5}$$

Where μ_{eff} is the mobility reduction parameter, μ_0 denotes the low-field mobility and θ is a fitting parameter roughly given by:

$$\theta = \left(\frac{10^{-7}}{t_{ox}}\right)V^{-1} \tag{1.6}$$

Where t_{ox} is gate oxide thickness [4], typical values of θ is about $0.25\ V^{-1}$.

In short-channel MOSFET, the drain current of a MOS transistor operating in saturation is given by;

$$I_D = \frac{\beta}{2}\frac{(V_{GS}-V_{TH})^2}{1+\theta(V_{GS}-V_{TH})} \tag{1.7}$$

According to equation (1.7), the term $(V_{GS} - V_{TH})$ voltage can be written as;

$$V_{GS}-V_{TH} = \frac{I_D\theta}{\beta}+\sqrt{\left(\frac{I_D\theta}{\beta}\right)^2+\frac{2I_D}{\beta}} \tag{1.8}$$

Since the drain current is in μA, then;

$$\left(\frac{I_D\theta}{\beta}\right)^2 \langle\langle \left(\frac{2I_D}{\beta}\right) \tag{1.9}$$

Using equation (1.9), equation (1.8) can be rewritten as;

$$V_{GS} - V_{TH} \approx \frac{I_D\theta}{\beta} + \sqrt{\frac{2I_D}{\beta}} \tag{1.10}$$

As a result, when using short-channel MOS transistors, ignoring the carrier mobility reduction will lead to error in the drain current and hence degrade the accuracy of the designed circuits. Consequently something has to be done to compensate for these errors.

This work will focus on the compensation of the error due to carrier mobility reduction in MOS translinear loop based analog computational circuits.

1.2 Current-mode Circuits Based on MTL Principle

MOSFET translinear loop (MTL) principle defined as a loop with an even number of transistors, with as many gate-source connections arranged clockwise as the number of gate-source connections in counterclockwise configuration. The MTL principle was developed by [5] and [6]. Circuits based on MTL using short-channel MOSFET suffer from second order effects such as channel length modulation, body effect and carrier mobility reduction. The effect of channel length modulation can be ignored if the supply voltage is reduced. Also the effect of body can be ignored if the source terminal is connected to the substrate. But, this is not the case for the reduction in carrier mobility. Something has to be done to cancel/minimize the error due to this effect, otherwise all

circuits designed using the MTL principle will have a poor accuracy. As an illustration of this effect, consider the four transistors translinear loop shown in Figure (1.4).

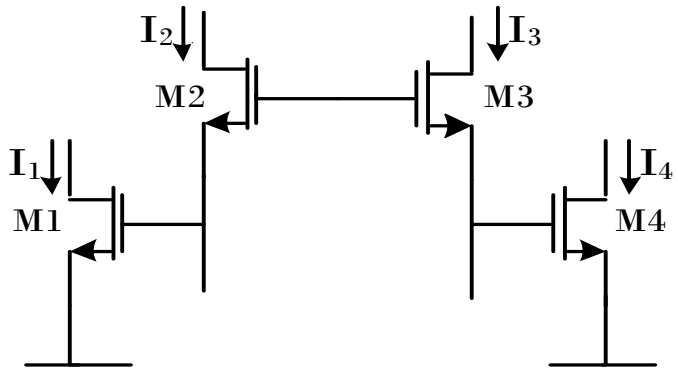

Figure 1.4 MTL loop

According to the MTL principle,

$$\sum_{cw} V_{GS} = \sum_{ccw} V_{GS} \tag{1.11}$$

Where the subscripts *cw* and *ccw* indicate the devices connected clockwise and counterclockwise in the loop respectively.

The loop voltages are given by:

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \tag{1.12}$$

Assuming the carrier mobility reduction and channel length modulation effects are ignored, the drain current equation of MOS transistors in the saturation region is given by:

$$I_D = \frac{\beta}{2}(V_{GS} - V_{TH})^2 \tag{1.13}$$

From equation (1.13), V_{GS} can be written as:

$$V_{GS} = \sqrt{\frac{2I_D}{\beta}} + V_{TH} \tag{1.14}$$

Substituting equation (1.14) into equation (1.12) and assuming matched transistors and neglecting the body effect, then;

$$\sqrt{I_{D1}} + \sqrt{I_{D2}} = \sqrt{I_{D3}} + \sqrt{I_{D4}} \tag{1.15}$$

Equation (1.15) is the main idea in the design of analog computational circuits. If the carrier mobility reduction is not ignored, which is the case for short-channel MOS transistor; equation (1.7) will be used.

It is clear from equation (1.16) that it is difficult to express V_{GS} as a closed form function of the drain current. Thus it is not possible to obtain an equation similar to equation (1.15). Consequently, it will not be possible to get an accurate computational circuit without compensating the error resulting from the carrier mobility reduction. The same problems apply to other current-mode circuits. This work will focus on developing a solution to cancel/minimize errors due to carrier mobility reduction and apply the proposed solution to some predesigned CMOS current-mode analog computational circuits.

1.3 Motivation

It is well known that scaling down transistor size reduced chip size, lower gate delays, allowing higher frequency operation and reduce the power consumption. Associated with these benefits some unwanted side effects known as second order effects are introduced. The carrier mobility reduction is one of these unwanted effects. The motivation of this thesis is to cancel/minimize the error in short-channel MOSFET circuits resulting from carrier mobility reduction to improve the accuracy in analog computational circuits designed based on MTL principle. Consequently the objective of this thesis is to design current-mode CMOS analog circuits such as (square-rooting circuit, squaring circuit and multiplying circuit) that are reduced the short-channel effect caused carrier mobility reduction.

1.4 Research Problem Statement

Many current mode CMOS analog computational circuits using MOSFET have been reported in the literature. Most of them were developed for long-channel, in which carrier mobility reduction is ignored, using simple long channel MOSFET model. This cannot be applied to short-channel MOS transistor because carrier mobility reduction of the MOS transistor changes with its gate-source voltage as stated previously.

In short channel MOS transistor, second order effects become more important and require modifications to the MOS models or a way to compensate for the errors due to these effects. In this thesis, a new method to minimize/cancel errors due to carrier mobility

reduction based on MTL is developed. Some CMOS current-mode analog computational circuits are designed using this approach.

1.5 Thesis Organization

The thesis is divided into four chapters and its outline is described as given below:

- **Chapter 1: Introduction.**

This chapter presents various types of second order effects, current-mode circuits based on MTL principle, motivation, research problem statement and the outline of thesis.

- **Chapter 2: Literature Review.**

Chapter 2 summarizes previous work of CMOS analog computational circuits such as square-rooting, a squaring and multiplying

- **Chapter 3: Design and Simulation of Current-Mode CMOS Analog Computational Circuits.**

In this chapter using the proposed technique, some CMOS analog computational circuits such as square-rooting, a squaring and multiplying are redesigned and simulated to overcome the errors of the output current caused by carrier mobility reduction.

- **Chapter 4: Conclusion and Future Work.**

Finally in Chapter 4, the thesis conclusion is provided along with recommended future studies and extensions.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The demand for low-voltage and low power current-mode circuit design has been widely increasing, especially for battery powered applications. However, high accuracy and large dynamic range over wide range frequencies of analog circuits are needed. The CMOS technology is the best choice for these requirements and is the desirable basis for the most complex analog signal processing. Therefore, CMOS analog computational circuits with nonlinear functions may greatly enhance signal processing capability such as waveform generation, fuzzy control, neural network, adaptive filtering, analog to digital (A/D) converter, RMS-averaging, frequency translation and modulation [7]–[12]. These circuits have been gained attention to be able to exploit the potential of current-mode analog signal processing, providing attractive and best solution for many circuits and system problems.

2.2 Analog Computational Circuits

A number of CMOS analog computational circuits such as square-rooting, squaring and multiplying circuits have been presented in many literatures [7]–[21]. Some of them are the voltage-mode[7], [16] and some other are the current-mode [8], [9]. In addition, analog computational circuits designed using MOSFET operating in strong inversion can

be classified based on the transistor mode of operation, linear [11], [17] and saturation [13]–[15]. There are different approaches used to design analog computational circuits. One approach is based on MOSFET translinear loop (MTL) and it is the most commonly used [18]–[21]. The starting point in designing such circuits is the use of the square-law drain current equation of the MOS transistor. This model can't be used in circuits designed using a short-channel MOS transistors, where second order effects should be considered. In the next section, literature survey on the previous work done in the design of some current mode analog computational circuits using MOSFET in strong inversion will be presented. More attention will be given to the compensation techniques used for the error caused by carrier mobility reduction.

2.2.1 Square-rooting Circuit

A square-rooting circuit is one of the useful analog building blocks used in measurement, instrumentation and neural networks [22]–[25]. For instance, it can be used to calculate the r.m.s value of an arbitrary waveform [22] and the Euclidean distance between two vectors [23]. In the past, the square-rooting circuit is realized using operational amplifiers (Op-Amp) and bipolar junction transistors (BJT) [26],[27]. The frequency performance of this approach is limited by the bandwidth of the Op-Amp. There are many voltage-mode and current-mode square-rooting circuit based on MOS transistors that are used in the implementation of several analog building blocks such as differentiators [28]–[30], integrators [31], oscillators [32]–[34], and filters [35]–[38]. The current mode geometric-mean has been realized using square-root-domain block [36], [37]. However, the current-mode multiplier-divider circuit has been realized using both geometric mean and squarer-

divider block [39], [40]. All the previously mentioned designs used the simple long-channel transistor model and hence, second order effects are ignored.

In addition, several CMOS square-rooting circuits were realized based on a square-law model of the MOS transistor operating in saturation region [41]–[51]. A new current-mode squaring circuit that reduces short-channel effect caused by carrier mobility reduction was proposed in [52] and is shown in Figure (2.1) . A transistor (M18) added between the gates of transistors M2 and M3 is used as an active resistor to compensate for error due to the carrier mobility reduction. In this case, the output current will flow through this transistor, so a new voltage term will be added to the MTL to cancel the error in the output. The drawback of this approach is that a controllable voltage (V_C) is required. Also, changes in the drain-source voltage (V_{DS}) of the transistor (M18) cause variations in the resistance value which degrades the accuracy of the circuit.

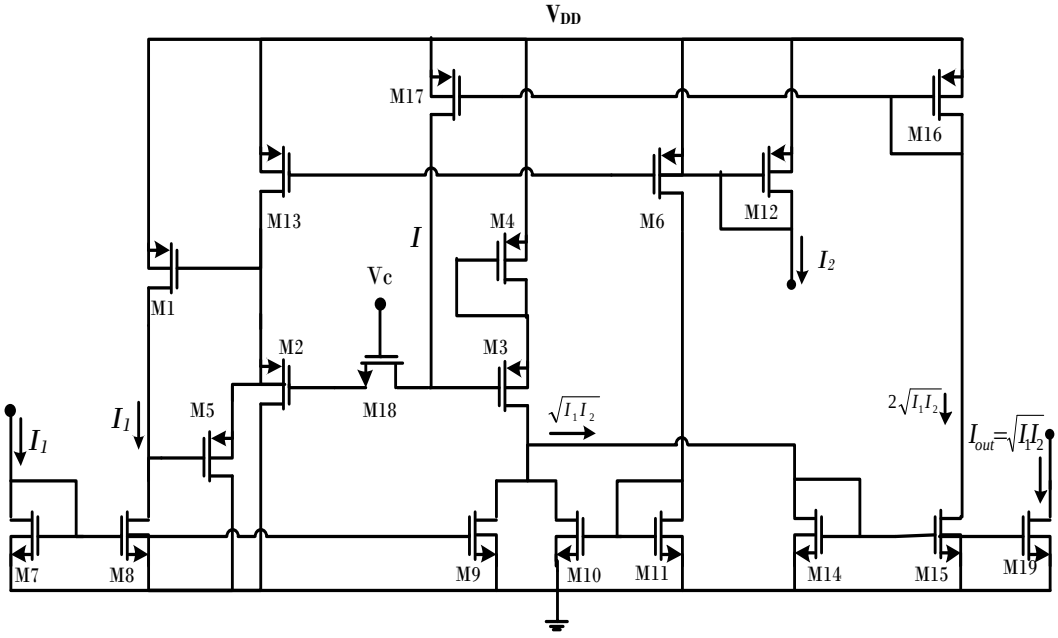

Figure 2.1 Current-mode MOS square-rooting circuit [52]

Table (2.1) summarizes the performance parameters for various CMOS square-rooting circuits designed using short-channel MOSFETs.

Table 2.1 Summary of various CMOS square-rooting circuits

Ref.	Public. Year	Type (In/Out)	Tech.	Supply Voltage	Input Range	Power Cons.	Relative Error	-3 dB Frequency	Area
[48]	2009	CI/CO	0.35 µm	3V	-	-	-	-	-
[49]	2009	CI/CO	0.18 µm	1.5V	40 µA	-	-	-	-
[50]	2010	CI/VO	0.25 µm	±0.7V	50 µA	1.4 (µW)	0.55%	-	-
[51]	2007	VI/CO	0.25 µm	1.8V	-	145 (µW)	2.5%	158 MHz	410µm^2
[52]	2007	CI/CO	0.35 µm	3.0V	10µA	-	1.26%	-	-

2.2.2 Squaring Circuit

The squaring circuit is another important building block used in analog signal processing applications, such as RMS-DC converters, pseudo-exponential cells, CMOS companding filters, fuzzy control, multipliers, …etc.[53]–[57].

Squaring circuits designed using MOSFETs in saturation can be classified in two categories. The first one is the direct approach using MTL [53], [58]. The second approach uses the analog multiplier to obtain the squaring output. This multiplier can be designed with MOS transistor operating in saturation region [59] or both saturation and triode region [60]. In [61] a CMOS current-mode squaring circuit is proposed and is shown in Figure (2.2). The main advantage of this approach it is insensitive to the threshold voltage variation caused by body effect, but this circuit suffers from error due to the carrier mobility reduction effect.

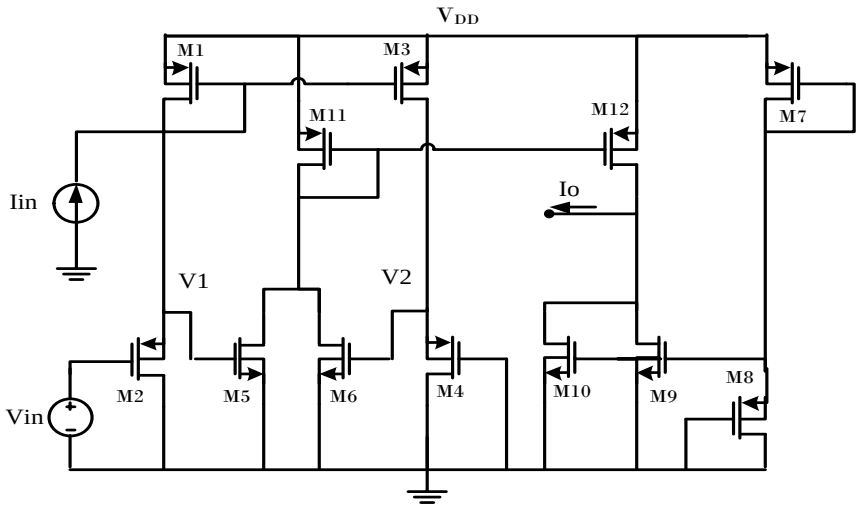

Figure 2.2 Current-mode MOS squaring circuit [61]

In reference [62], a new current-mode squaring circuit that reduces short-channel effect caused by carrier mobility reduction was proposed and is depicted in Figure (2.3). This approach used the same approach presented in reference [52] to compensate for the carrier mobility reduction, so it has the same drawbacks that is mentioned regarding the circuit in reference [52].

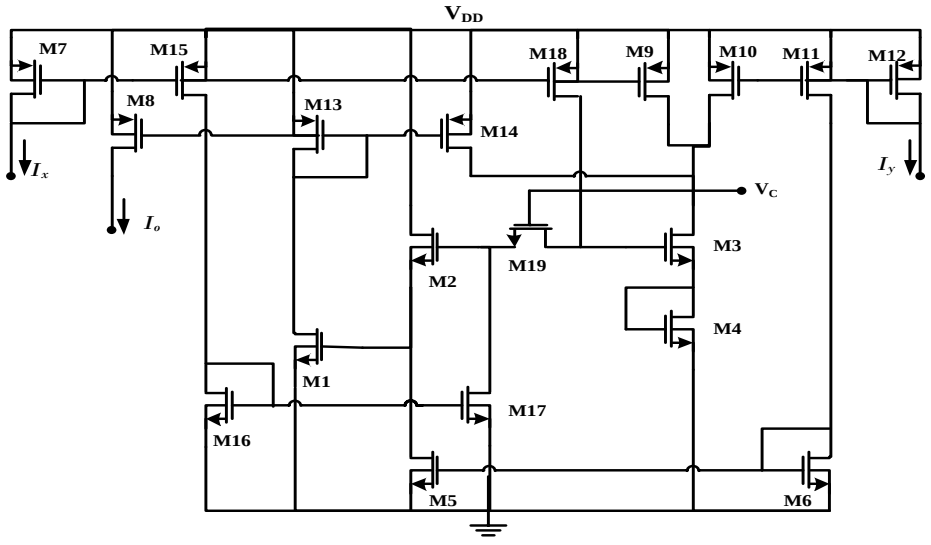

Figure 2.3 Current-mode MOS squaring circuit [62]

In [63] a high precision MOS translinear loop based squarer/divider circuit free from mobility reduction is proposed. In this approach, small resistor is added in the MTL path to compensate for the error due to carrier mobility reduction as shown in Figure (2.4). The main drawbacks of this design are the increase in the silicon area and the power consumption of the circuit.

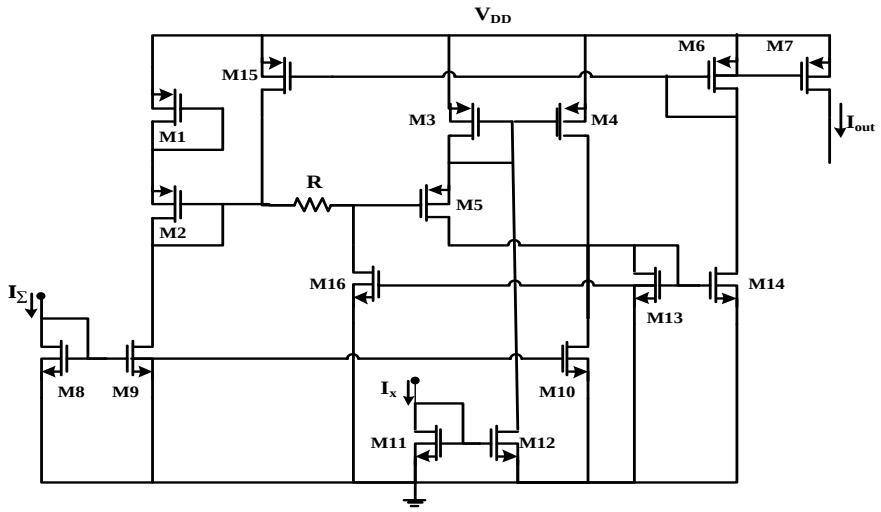

Figure 2.4 Current-mode MOS squaring circuit [63]

The summary of the performance parameters of various MOS squaring circuits using short-channel MOSFET is listed in Table (2.2)

Table 2.2 Comparison of different CMOS squaring circuits in short-channel

Ref.	Public. Year	Type (In/Out)	Tech.	Supply Voltage	Input Range	Power Cons.	Relative Error	-3 dB Frequency	Area
[51]	2008	VI/CO	0.25µm	3.3V	±1.0 V	90µW	3%	200MHz	340(µm^2)
[61]	2011	CI/CO	0.25µm	1.4V	±40µA	72.6µW	1.9%	0.03MHz	-
[62]	2007	CI/CO	0.35µm	3V	7µA	-	-	50MHz	1500(µm^2)
[63]	2011	CI/CO	0.35µm	-	40µA	-	-	-	-

2.2.3 Multiplying Circuit

Analog multiplying is a basic building block used in many analog signal processing applications such as adaptive equalization, waveform generation, modulators, phase detectors, and other signal processing circuits [64]–[69]. The main performance properties of the required multiplying function are accuracy, wide bandwidth, large dynamic range, low supply voltage, low power and low distortion. The most famous bipolar analog multiplying design is reported by Gilbert [70], [71]. A CMOS version of Gilbert cell based multiplier is reported in [72], [73]. Recently, some work has been carried out in the area of CMOS analog multiplier design [74]–[76]. Square-law model of the MOS transistor operating in the saturation region is used to realize these circuits. Also, some of CMOS multiplying circuits were designed using MOS transistors operating in the linear region [77]–[79].

Several CMOS multiplying circuits were designed using short-channel MOSFET but they didn't compensate for the error due to carrier mobility reduction [20], [51], [61], [80]–[82]. Therefore, the accuracy of these circuits is degraded. A few CMOS analog multiplying circuit ware designed to reduce the second order effects such as body effect [61] and carrier mobility reduction [83]–[86] or both [85].

In [84], [85] a CMOS analog multiplier free from carrier mobility reduction is proposed. With reference to Figure (2.5), the input cell is formed by transistors M1-M4 which have the same fixed gate-source voltage. Hence, the linearity of the CMOS analog multiplier is independent of the mobility reduction. The main disadvantage of these approaches is that circuits are voltage-mode; therefore dynamic range will be limited.

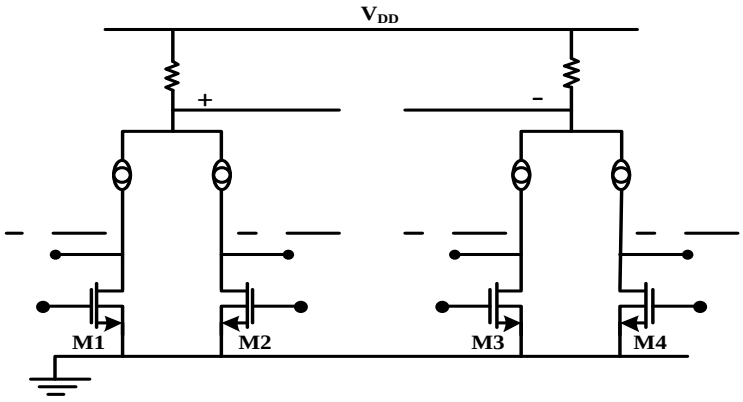

Figure 2.5 Multiplier cell [85]

In reference [86] a novel high-precision current-mode multiplier/divider is proposed. This multiplier was designed based on both square-rooting and squaring circuits as depicted in Figure (2.6). Two resistors R1 and R2 are used in the MTL path to compensate for the error due to carrier mobility reduction. These resistors increase the silicon area and the power consumption of the circuit.

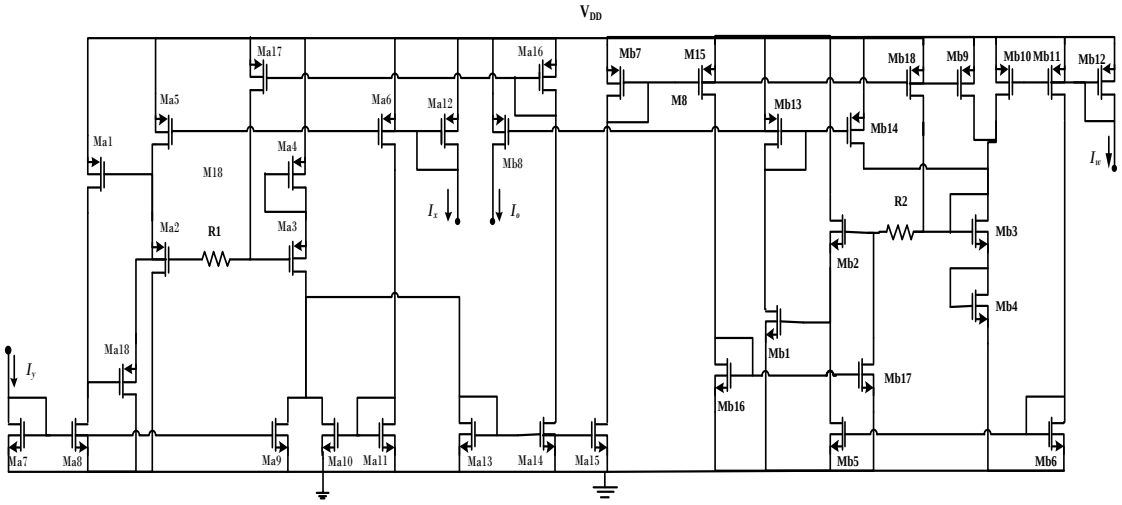

Figure 2.6 Current-mode MOS multiplying circuit [86]

Table (2.3) summarizes the performance parameters of various multiplying circuits designed using short-channel MOSFETs.

Table 2.3 Summary of various CMOS multiplying circuits in short-channel

Ref.	Public. Year	Type (In/Out)	Tech.	Supply Voltage	Input Range	Power Cons.	Relative Error	-3 dB Frequency	Area
[20]	2009	CI/CO	0.35µm	3.3V	±10µA	240µW	1.15%	44.9MHz	-
[61]	2011	CI/CO	0.25µm	1.4V	7µA	32.4µW	-	249MHz	-
[80]	2009	CI/CO	0.35µm	3.3V	±10µA	340µW	1.1%	41.8MHz	-
[81]	2010	CI/CO	0.35µm	1.5V	±20µA	1010µW	6.4%	343MHz	18603µm^2
[82]	2012	CI/CO	0.25µm	2.5V	±10µA	168µW	-	278MHz	331.5µm^2
[86]	2009	CI/CO	0.35µm	3V	10µA	-	-	44MHz	10000µm^2

2.3 Conventional Analog Computational Circuits

In this section, the conventional current-mode design of square-rooting, squaring and multiplying circuits will be explained. These cells will be used as a core cells in the proposed designs. More detail about every design will be given in the next sections.

2.3.1 Square-rooting Circuit

The conventional current-mode square-rooting circuit also known as geometric mean cell have two inputs (I_1 , I_2) and one output ($I_{out} = \sqrt{I_1 I_2}$) as shown in Figure (2.7).

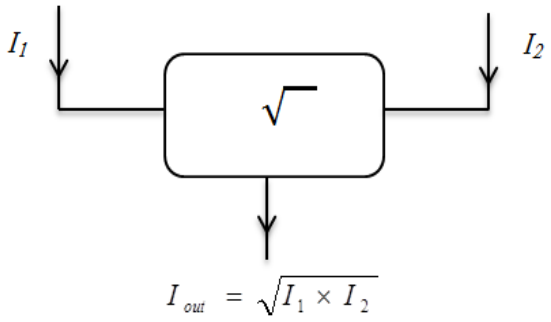

Figure 2.7 Block diagram of the current-mode square-rooting circuit

In [52] a conventional current-mode square-rooting circuit is reported and is shown in Figure (2.8). Assuming the aspect ratios of transistors M1-M4 are chosen to be $\beta_1 = \beta_2 = \beta$ and $\beta_3 = \beta_4 = 2\beta$ where β is the trasconductance parameter of the pMOS transistor. Appling MTL around transistors M1-M4 yield:

$$V_{SG1} + V_{SG2} = V_{SG3} + V_{SG4} \tag{2.1}$$

Assuming that the carrier mobility reduction and channel length modulation effects are ignored, the drain current of the transistor in the saturation region is given by:

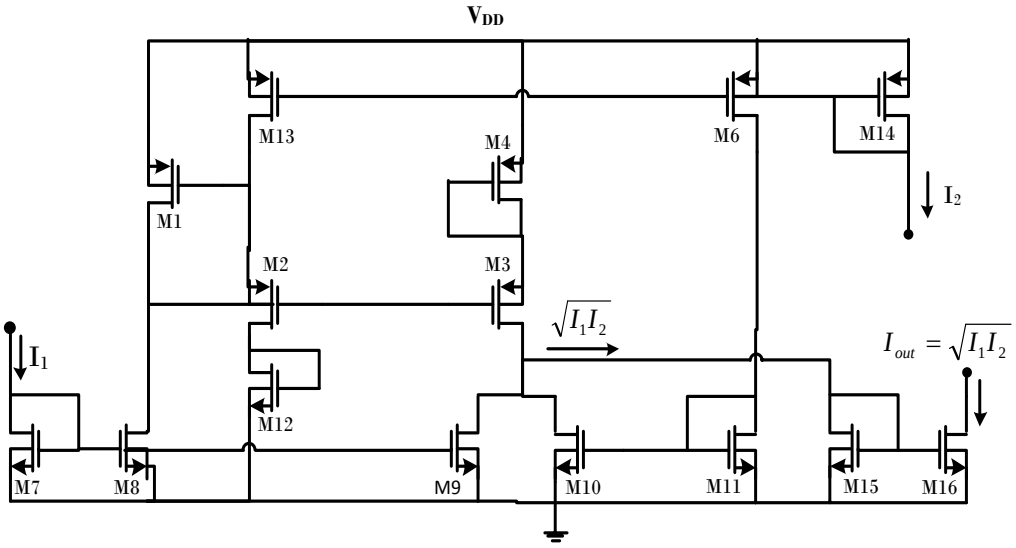

Figure 2.8 Conventional current-mode square-rooting circuit [52]

$$I_D = \frac{\beta}{2}(V_{GS} - V_{TH})^2 \tag{2.2}$$

From equation (2.2), V_{GS} can be written as:

$$V_{GS} = \sqrt{\frac{2I_{Di}}{\beta}} + V_{TH} \tag{2.3}$$

Where I_{Di} is the drain current in the transistor M_i;

Combining equations (2.1) and (2.3) and assuming all transistors are identical and neglecting body effect the following equation is obtained:

$$\sqrt{2I_{D1}} + \sqrt{2I_{D2}} = \sqrt{I_{D3}} + \sqrt{I_{D4}} \tag{2.4}$$

According to Figure (2.8), the drain current of M3 and M4 are the same and squaring both sides of equation (2.4), the drain current of M3 can be expressed as:

$$I_3 = \sqrt{I_1 I_2} + \frac{1}{2}(I_1 + I_2) \tag{2.5}$$

The second term to the right of equation (2.5) is canceled by proper selection of the aspect ratios for M9 and M10, so the output current is given by:

$$I_{out} = I_3 - \frac{1}{2}(I_1 + I_2) = \sqrt{I_1 I_2} \tag{2.6}$$

Equation (2.6) confirms that the output current I_{out} is the square-root of the multiplying input currents (I_1, I_2).

2.3.2 Squaring Circuit

A conventional current-mode squaring circuit based on MTL is proposed in [44] and is shown in Figure (2.9). The aspect ratios of transistors M1- M4 are selected such that $\beta 1 = \beta_2 = 2\beta$ and $\beta_3 = \beta_4 = \beta$ where β is the trasconductance parameter of the PMOS transistor. Writing MTL around transistors M1- M4, then:

$$V_{SG1} + V_{SG2} = V_{SG3} + V_{SG4} \tag{2.7}$$

Assuming matched transistors and neglecting the second order effects are negligible. The following equation can be obtained:

$$\sqrt{\frac{2I_{D1}}{2\beta}} + \sqrt{\frac{2I_{D2}}{2\beta_2}} = \sqrt{\frac{2I_{D3}}{\beta}} + \sqrt{\frac{2I_{D5}}{\beta}} \tag{2.8}$$

where I_{Di} is the drain current in transistor *Mi*;

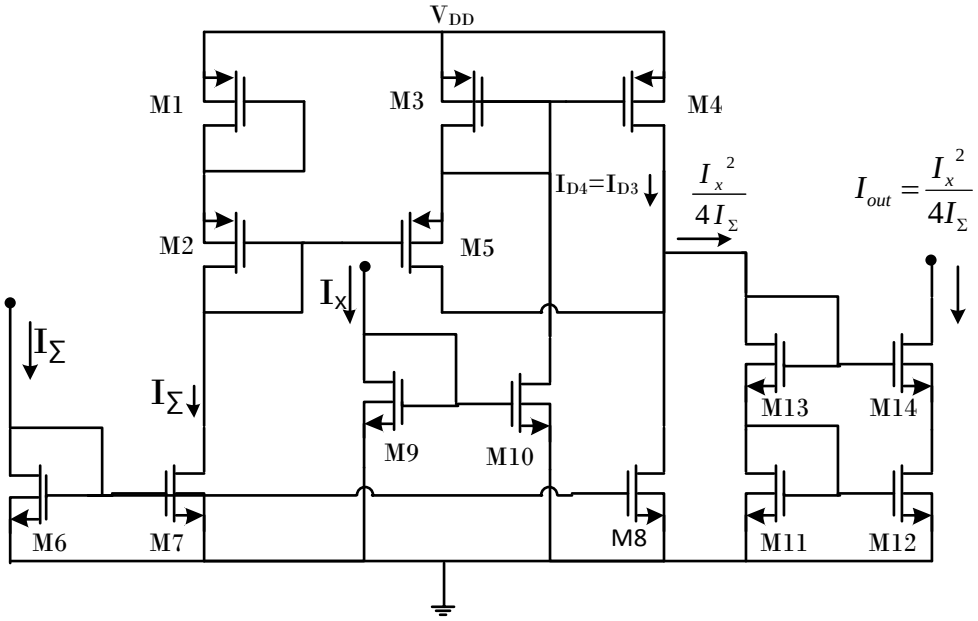

Figure 2.9 Conventional current-mode squaring circuit [44]

According to Figure (2.9), the drain currents of M1 and M2 are the same and equal I_{Σ}, the equation (2.8) can be rewritten as:

$$\sqrt{2I_{D5}} = 2\sqrt{I_{\Sigma}} - \sqrt{2I_{D3}} \tag{2.9}$$

If the following condition is imposed:

$$I_{D3} = I_X + I_{D5} \tag{2.10}$$

Combining equations (2.9) and (2.10) and squaring the result for twice, the drain current for M5 is given by:

$$I_{D5} = \frac{I_\Sigma}{2} - \frac{I_x}{2} + \frac{I_x^{\,2}}{8I_\Sigma} \tag{2.11}$$

According to the circuit schematic in Figure (2.9), the output current of the circuit is:

$$I_{out} = I_{D4} + I_{D5} - I_\Sigma \tag{2.12}$$

Combining equations (2.11) and (2.12) to get:

$$I_{out} = \frac{I_x^{\,2}}{4I_\Sigma} \tag{2.13}$$

Equation (2.13) confirms that the output current I_{out} is the square of the input current I_x.

2.3.3 Multiplying Circuit

A conventional current-mode multiplying circuit can be obtained in two ways. The first way is based on both square-rooting and squaring circuits as depicted in Figure (2.10) [87]. The output current is given by:

$$I_{out} = \frac{I_{in}^2}{I_w} = \frac{\left(\sqrt{I_x I_y}\right)^2}{I_w} = \frac{I_x I_y}{I_w} \tag{2.14}$$

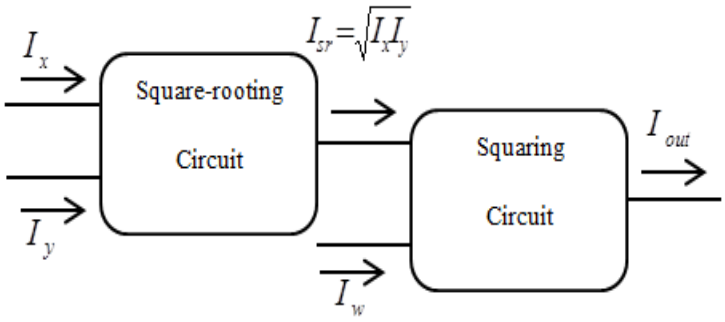

Figure 2.10 Block diagram of the multiplying circuit [87]

The other way to obtain multiplying circuit is based on two squaring circuits and one subtracting circuit as illustrated in Figure (2.11). It is easy to show that the output current is given by:

$$I_{out} = (I_x + I_y)^2 - (I_x - I_y)^2 = 4I_x I_y \qquad (2.15)$$

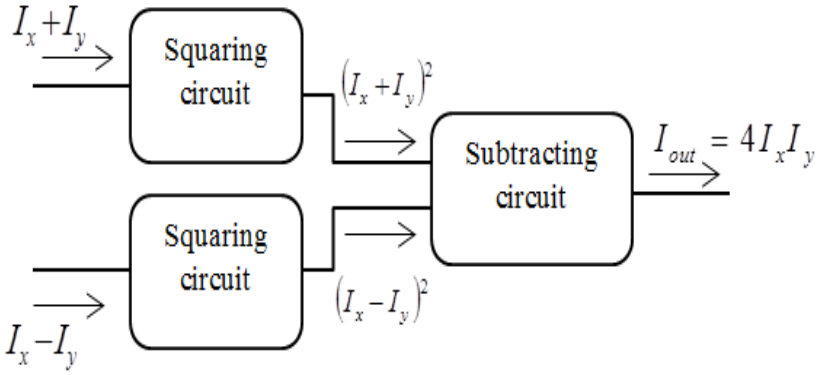

Figure 2.11 Block diagram of the multiplying circuit

The main advantage of using the square-difference identity in the multiplying circuit is to cancel the offset error. In order to implement a current-mode multiplying circuit, two squaring and subtracting circuits must be designed. According to Figure (2.11), if the

input current is (I_x+I_y) or (I_x-I_y) instead of I_x, the output current can be expressed as:

$$I_{O1} = \frac{(I_x + I_y)^2}{4I_\Sigma} \quad or \quad I_{O2} = \frac{(I_x - I_y)^2}{4I_\Sigma}.$$

With the reference to Figure (2.11), the output current of the multiplying circuit is:

$$I_{out} = I_{O1} - I_{O2} = \frac{(I_x + I_y)^2}{4I_\Sigma} - \frac{(I_x - I_y)^2}{4I_\Sigma} \tag{2.16}$$

It is easy to show that the output current is given by:

$$I_{out} = \frac{I_x I_y}{I_\Sigma} \tag{2.17}$$

It is clear that, all the above circuits didn't consider the cancellation of the error due to carrier mobility reduction which degrades the accuracy of these circuits.

2.4 Research Goals

The main objective of this work is to investigate the feasibility of finding solutions for reducing/cancelling errors due to carrier mobility reduction in short-channel MOSFETs operating in strong inversion. Using this proposed technique, some analog computational circuits such as square-rooting, a squaring and multiplying will be redesigned and simulated.

CHAPTER 3

DESIGN AND SIMULATION OF CURRENT-MODE CMOS ANALOG COMPUTATIONAL CIRCUITS

3.1 Introduction

As stated before, second order effect in short-channel MOSFET will degrade the accuracy of the design. In this work, CMOS conventional current-mode that consisted of square-rooting circuit, squaring circuit and multiplying circuit using MTL principle in strong inversion are redesigned to minimize the errors generated by carrier mobility reduction. The proposed circuits that would be adopted must have a good linearity, small silicon area, low power supply, low power consumption and wide bandwidth.

3.2 Current-mode Square-rooting Circuit

In this section, the proposed current-mode square-rooting circuit will be discussed. However, simulation results and mismatch analysis will be carried out. Summary of performance comparison will be given as well.

3.2.1 Proposed Current-mode Square-rooting Circuit

The proposed current-mode square-rooting circuit using short-channel MOSFETs with compensation for error resulting from carrier mobility reduction is realized. The

conventional current-mode square-rooting circuit which is given in Figure (2.8) is modified as shown in Figure (3.1).

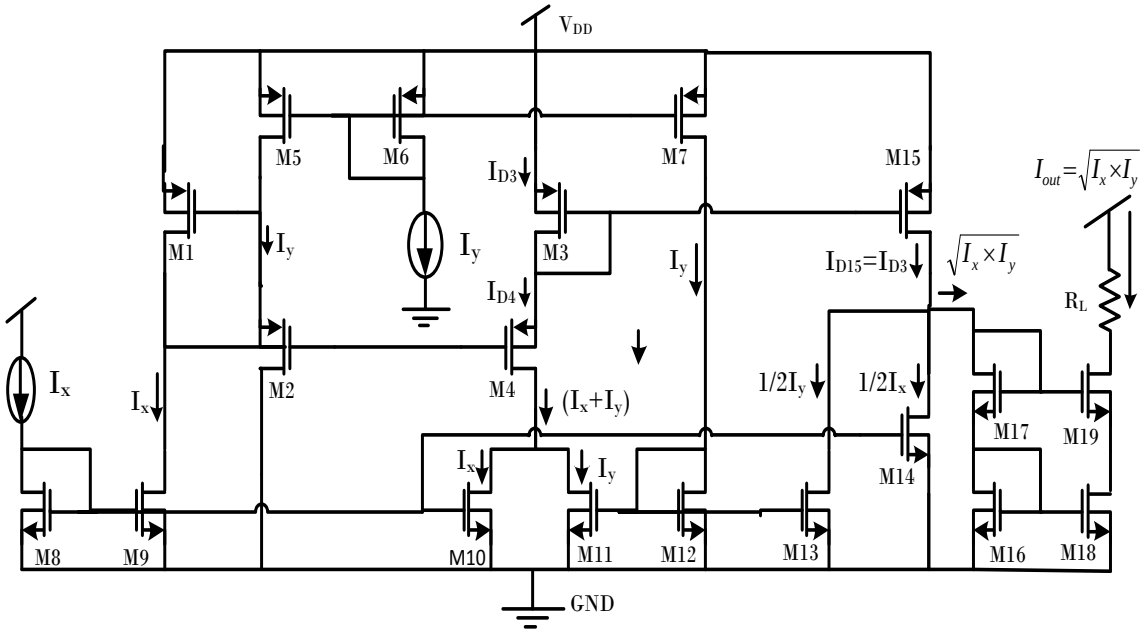

Figure 3.1 Proposed current-mode CMOS square-rooting circuit

With the reference to the Figure (3.1), the input current can be applied via M6 as I_y or via M8 as I_x. If the input current is negative, use I_y as the input and I_x as a bias current and vice versa.

Writing MTL around transistors M1-M4 to get:

$$V_{SG1} + V_{SG2} = V_{SG3} + V_{SG4} \tag{3.1}$$

If the carrier mobility reduction is taken into consideration, the MOS drain current is given by:

$$I_D = \frac{\beta}{2} \frac{(V_{GS} - V_{TH})^2}{1 + \theta(V_{GS} - V_{TH})} \tag{3.2}$$

Where, θ is a fitting parameter and β is the transconductance of the MOSFET.

With reference to equation (1.10), it is easy to show that:

$$V_{GS} \approx \frac{I_D \theta}{\beta} + \sqrt{\frac{2I_D}{\beta}} + V_{TH} \tag{3.3}$$

Combining equations (3.1) and (3.3) to get:

$$\frac{I_{D1}\theta_1}{\beta_1} + \sqrt{\frac{2I_{D1}}{\beta_1}} + \frac{I_{D2}\theta_2}{\beta_2} + \sqrt{\frac{2I_{D2}}{\beta_2}} = \frac{I_{D3}\theta_3}{\beta_3} + \sqrt{\frac{2I_{D3}}{\beta_3}} + \frac{I_{D4}\theta_4}{\beta_4} + \sqrt{\frac{2I_{D4}}{\beta_4}} \tag{3.4}$$

where, I_{Di} is the drain current for transistor M_i. Assuming that $\beta_1 = \beta_2 = \beta$, $\beta_3 = \beta_4 = 2\beta$, and $\theta_1 = \theta_2 = \theta_3 = \theta_4 = \theta$. With the reference to Figure (3.1), $I_{D1} = I_x$ and $I_{D2} = I_y$, then equation (3.4) can be rewritten as:

$$\frac{I_x\theta}{\beta} + \sqrt{\frac{2I_x}{\beta}} + \frac{I_y\theta}{\beta} + \sqrt{\frac{2I_y}{\beta}} = \frac{I_{D3}\theta}{2\beta} + \sqrt{\frac{I_{D3}}{\beta}} + \frac{I_{D4}\theta}{2\beta} + \sqrt{\frac{I_{D4}}{\beta}} \tag{3.5}$$

Since the drain current of transistors M3 and M4 are the same, equation (3.5) can written as:

$$\frac{\theta}{\beta}(I_x + I_y) + \frac{1}{\sqrt{\beta}}\left(\sqrt{2I_x} + \sqrt{2I_y}\right) = \frac{\theta}{\beta} I_{D3} + \frac{2}{\sqrt{\beta}}\sqrt{I_{D3}} \tag{3.6}$$

If we force the following condition:

$\frac{\theta}{\beta}(I_x + I_y) = \frac{\theta}{\beta} I_{D3}$, then;

$$I_{D3} = I_x + I_y \tag{3.7}$$

Combining equations (3.6) and (3.7) to get:

$$\frac{1}{\sqrt{\beta}}\left(\sqrt{2I_x} + \sqrt{2I_y}\right) = \frac{2}{\sqrt{\beta}}\sqrt{I_{D3}} \tag{3.8}$$

Squaring both side of equation (3.8) to get:

$$2(I_x + I_y) + 4\sqrt{I_x I_y} = 4I_{D3} \tag{3.9}$$

Equation (3.9) can be rewritten as:

$$I_{D3} = \sqrt{I_x I_y} + \frac{I_x + I_y}{2} \tag{3.10}$$

The second term to the right of equation (3.10) is subtracted using M13 and M14 as shown in Figure (3.1), then the output current is given by:

$$I_{out} = \sqrt{I_x \times I_y} \tag{3.11}$$

If the current I_y is kept fixed, equation (3.11) can be rewritten as:

$$I_{out} = K\sqrt{I_x} \tag{3.12}$$

Where $K = \sqrt{I_y}$

It is clear that equation (3.12) implements square-rooting circuit that is free of errors due to carrier mobility reduction.

However, the proposed circuit shown in Figure (3.1) uses basic MOS current mirrors. In such mirrors, it is easy to examine the effect of the carrier mobility reduction. For example, transistors M8 and M9 form a current mirror. The drain current of transistors M8 and M9 can be written as:

$$I_{D8} = \frac{k'_n}{2}\frac{W}{L}\frac{(V_{GS8} - V_{TH})^2}{1 + \theta_8(V_{GS8} - V_{TH})} \tag{3.13}$$

$$I_{D9} = \frac{k'_n}{2}\frac{W}{L}\frac{(V_{GS9} - V_{TH})^2}{1 + \theta_9(V_{GS9} - V_{TH})} \tag{3.14}$$

But $V_{GS8}=V_{GS9,}$ and assuming $\theta_8= \theta_9$, the ratio of the drain currents of M8 and M9 is given by:

$$\frac{I_{D9}}{I_{D8}} = \frac{\left(\frac{k'_n}{2}\frac{W}{L}\frac{(V_{GS9}-V_{TH})^2}{1+\theta(V_{GS9}-V_{TH})}\right)}{\left(\frac{k'_n}{2}\frac{W}{L}\frac{(V_{GS8}-V_{TH})^2}{1+\theta(V_{GS8}-V_{TH})}\right)} = 1 \qquad (3.15)$$

Equation (3.15) can be rewritten as:

$$I_{D9} = I_{D8} \qquad (3.16)$$

This means there is no carrier mobility reduction error coming from current mirrors.

3.2.2 Simulation Results

The proposed square-rooting circuit was simulated using Tanner T-Spice in 0.18µm CMOS technology. The circuit is operating from *2V* power supply. The aspect ratios of all transistors used for simulation are listed in table (3.1). The bias current I_y is *3µA* and the input current I_x is swept from *0 to 80µA*. The output current was measured by forcing it through a load resistor $R_L=10k\Omega$.

Table 3.1 Transistors aspect ratio used in square-rooting circuit

W/L (µm)		W/L (µm)		W/L (µm)		W/L (µm)	
M1	2.5/0.35	M6	5.0/0.35	M11	5.0/0.35	M16	1.0/0.35
M2	2.5/0.35	M7	5.0/0.35	M12	5.0/0.35	M17	1.0/0.35
M3	5.0/0.35	M8	5.0/0.35	M13	2.5/0.35	M18	1.0/0.35
M4	5.0/0.35	M9	5.0/0.35	M14	2.5/0.35	M19	1.0/0.35
M5	5.0/0.35	M10	5.0/0.35	M15	5.0/0.35		

The DC transfer characteristic of the square-rooting circuit is shown in Figure (3.2). The figure shows the results for calculated and simulated result for both the conventional and the proposed design. It is clear from the figure that the simulated result for the proposed design is in a good agreement with calculated result. Plot of the error between calculated and simulated results is shown in Figure (3.3). It is clear that, the maximum relative error is 0.8%. The simulated maximum power consumption for the proposed circuit is $22.5\mu W$.

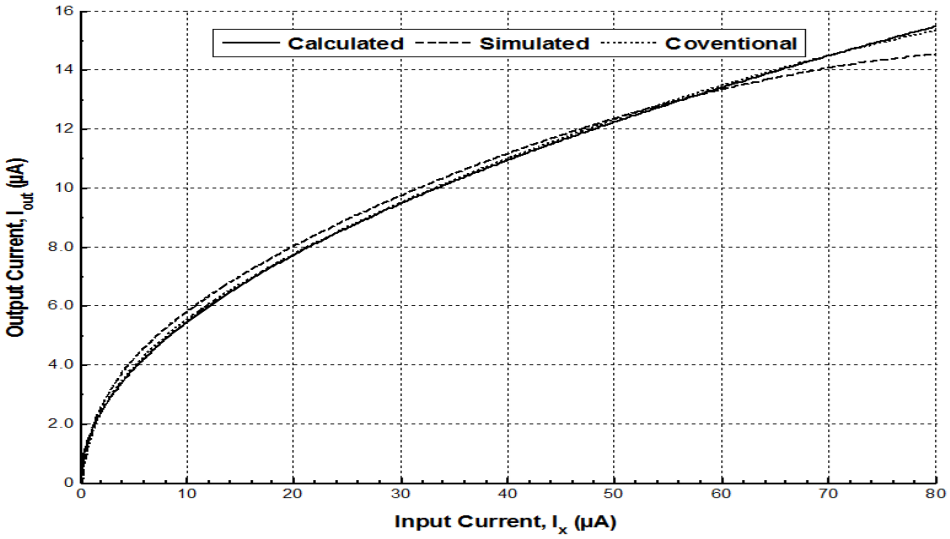

Figure 3.2 Simulated and calculated results for the square-rooting circuit

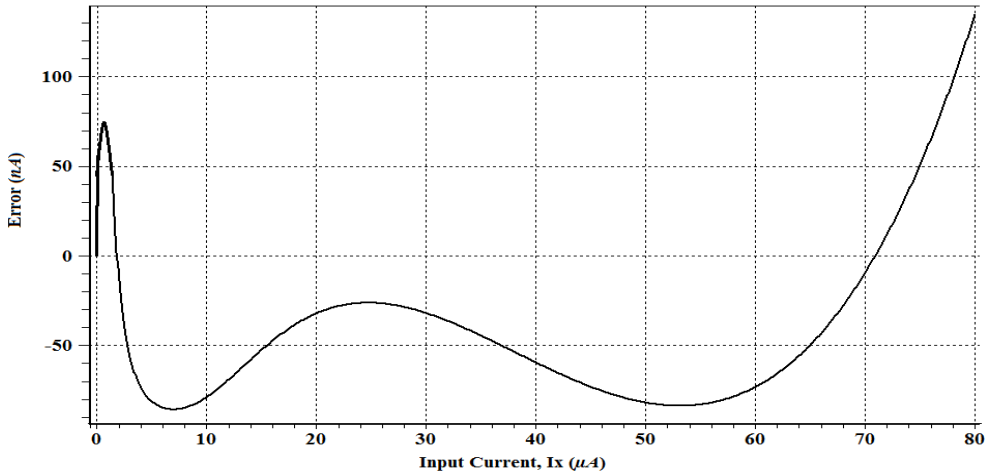

Figure 3.3 Simulation result for error of DC analysis

Figure (3.4) shows the output current of the proposed circuit when the input current is triangular with *80μA* peak and *1 kHz* frequency. It is clear that simulated and calculated results are in a good agreement as well.

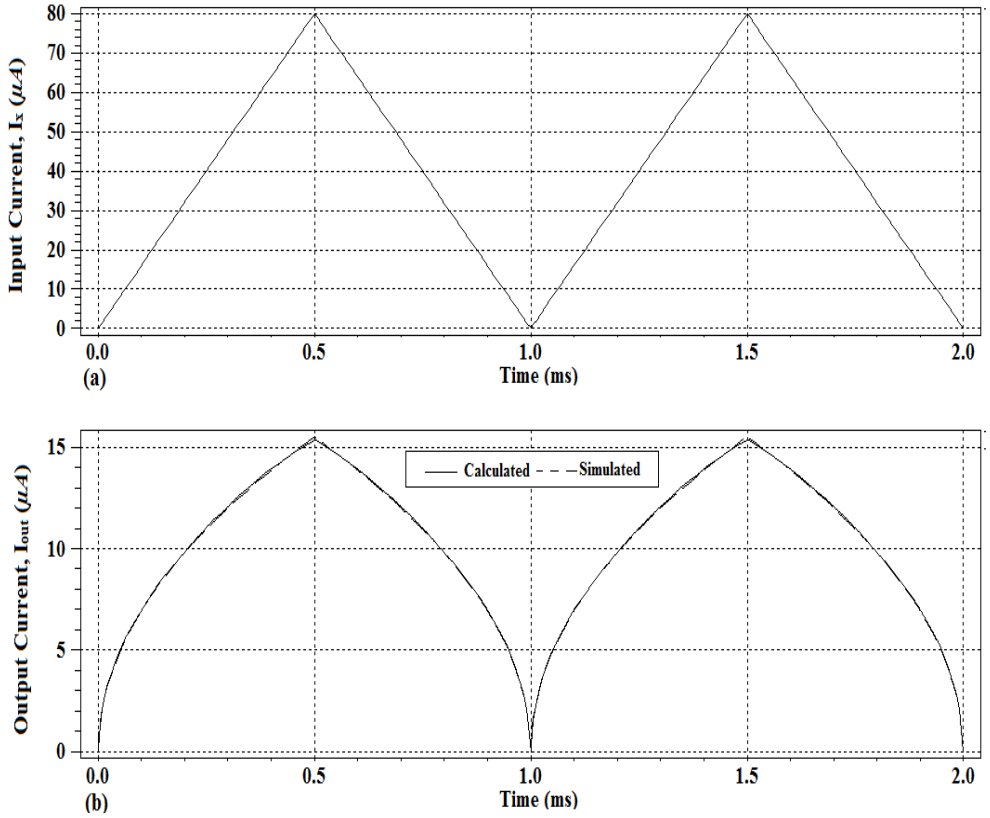

Figure 3.4 Simulation for transient analysis of the square-rooting circuit (a) Input signal (b) Output signal

However the circuit was simulated for temperature variation. The temperature was swept from -25°C to 75°C in steps of 50°C and the current was compared. The simulation result shown in Figure (3.5) appears that the output currents at *Ix* equal to *80μA* was *15.2μA*, *15.4μA* and *15.8μA* for temperatures equal to -25°C, 25°C and 75°C respectively while the calculated value is $\sqrt{(3\times10^{-6}\times80\times10^{-6})}=15.49\mu A$. The maximum deviation from the calculated value is *0.31μA* (2%) which happened at 75. In other words, the max deviation

is *0.004 μA* per 1°C. This means that the proposed circuit is a little sensitive to temperature variation.

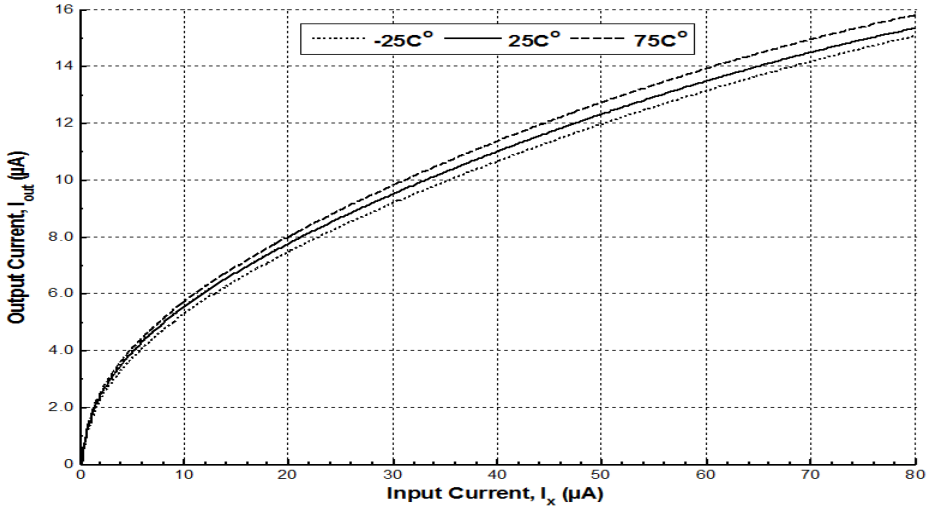

Figure 3.5 Simulation result for temperature variation of the square-rooting circuit

The proposed square-rooting circuit was simulated for the frequency response. An AC input signal is applied to I_x with *3μA* and the frequency is swept from 10Hz to 10GHz. Simulation result shown in Figure (3.6) indicates the -3dB frequency is *216MHz*.

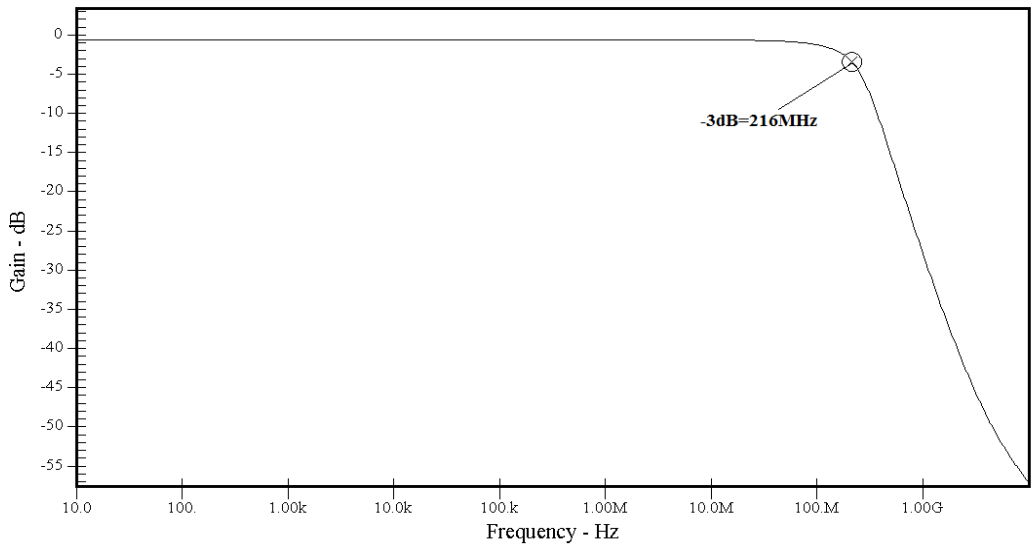

Figure 3.6 Frequency response of the proposed square-rooting circuit

3.2.3 Mismatch Analysis

The proposed square-rooting circuit was analyzed based on the assumption that the mobility parameter, transconductance parameter, threshold voltage and the channel length of transistors are matched. In this section, the influence of mismatch of these parameters in the MTL of the proposed circuit will be analyzed. Also, mismatch of threshold voltage and channel length of transistors in current mirrors of the proposed circuit will be discussed.

3.2.3.1 Mobility Parameter Mismatch

If it is assumed that the mobility parameters of transistors M1-M4 of the proposed square-rooting circuit are not perfectly matched such that:

$$\theta_1 = \theta_2 = \theta + \Delta\theta \tag{3.17}$$

$$\theta_3 = \theta_4 = \theta - \Delta\theta \tag{3.18}$$

where θ is the mobility parameter of transistors M1-M4 and $\Delta\theta$ is the mismatch term, then assuming perfect match on all other parameters, equation (3.6) can be rewritten as:

$$\frac{(\theta+\Delta\theta)}{\beta}(I_x + I_y) + \frac{1}{\sqrt{\beta}}\left(\sqrt{2I_x} + \sqrt{2I_y}\right) = \frac{(\theta-\Delta\theta)}{\beta} I_{D3} + \frac{2}{\sqrt{\beta}}\sqrt{I_{D3}} \tag{3.19}$$

Following the same analysis as before, it is easy to show that:

$$\frac{2\Delta\theta}{\sqrt{\beta}}(I_x + I_y) + \left(\sqrt{2I_x} + \sqrt{2I_y}\right) = 2\sqrt{I_{D3}} \tag{3.20}$$

If both sides are squared and the higher order terms are ignored, the drain current of M3 is given by:

$$I_{D3} = \sqrt{I_x I_y} + \frac{I_x + I_y}{2} + \frac{\Delta\theta}{\sqrt{\beta}}\left(I_x + I_y\right)\left(\sqrt{2I_x} + \sqrt{2I_y}\right) \tag{3.21}$$

The second term to the right of equation (3.21) is subtracted using transistors M13 and M14 and the output current is given by:

$$I'_{out} = \sqrt{I_x I_y} + \frac{\Delta\theta}{\sqrt{\beta}}\left(I_x + I_y\right)\left(\sqrt{2I_x} + \sqrt{2I_y}\right) \tag{3.22}$$

which results in an absolute error given by:

$$I_{error} = \left|I_{out} - I'_{out}\right| = \left|\frac{\Delta\theta}{\sqrt{\beta}}\left(I_x + I_y\right)\left(\sqrt{2I_x} + \sqrt{2I_y}\right)\right| \tag{3.23}$$

To evaluate the error due to mobility parameter mismatch using equation (3.23), consider the worst case where I_x=80μA, I_y=3μA, β=86μA/V^2, θ=0.25V^{-1} and ($\Delta\theta$=1% of θ) =0.0025V^{-1}, then the maximum error is 0.337μA which increase the error to 2.2%. This deviation confirms that the proposed circuit has acceptable range with the carrier mobility parameter mismatch.

3.2.3.2 Transconductance Parameter Mismatch

The same analysis can be performed on the transconductance parameter, $\beta_1 = \beta_2 = \beta - \Delta\beta$ and $\beta_3 = \beta_4 = \beta + \Delta\beta$, where β is the transconductance parameter value of transistors M1-M4 and $\Delta\beta$ is the mismatch term, then assuming perfect matching on all other parameters, the equation (3.6) can be rewritten as:

$$\frac{\theta}{(\beta-\Delta\beta)}(I_x+I_y)+\frac{1}{\sqrt{(\beta-\Delta\beta)}}\left(\sqrt{2I_x}+\sqrt{2I_y}\right)=\frac{\theta}{(\beta+\Delta\beta)}I_{D3}+\frac{2}{\sqrt{(\beta+\Delta\beta)}}\sqrt{I_{D3}} \qquad (3.24)$$

Following the same analysis as before, it is easy to show that:

$$\left\{\begin{array}{l}\frac{\theta}{\beta}\left(\frac{1}{1-\frac{\Delta\beta}{\beta}}\right)(I_x+I_y)-\frac{\theta}{\beta}\left(\frac{1}{1+\frac{\Delta\beta}{\beta}}\right)(I_x+I_y)\\ +\frac{1}{\sqrt{\beta}}\left(\sqrt{\frac{1}{1-\frac{\Delta\beta}{\beta}}}\right)\left(\sqrt{2I_x}+\sqrt{2I_y}\right)\end{array}\right\}=\frac{2}{\sqrt{\beta}}\left(\sqrt{\frac{1}{1+\frac{\Delta\beta}{\beta}}}\right)\sqrt{I_{D3}} \qquad (3.25)$$

It is well known that $\left(\frac{1}{1+x}\approx 1-x\right)$ if $(x<<1)$. Using this approximation in equation (3.25) to get:

$$\left\{\begin{array}{l}\frac{\theta}{\beta}\left(1+\frac{\Delta\beta}{\beta}\right)(I_x+I_y)-\frac{\theta}{\beta}\left(1-\frac{\Delta\beta}{\beta}\right)(I_x+I_y)+\\ \frac{1}{\sqrt{\beta}}\left(\sqrt{\left(1+\frac{\Delta\beta}{\beta}\right)}\right)\left(\sqrt{2I_x}+\sqrt{2I_y}\right)\end{array}\right\}=\frac{2}{\sqrt{\beta}}\left(\sqrt{\left(1-\frac{\Delta\beta}{\beta}\right)}\right)\sqrt{I_{D3}} \qquad (3.26)$$

But $\left(\frac{\Delta\beta}{\beta}<<1\right)$, then equation (3.26) can be rewritten as:

$$\frac{2\theta\Delta\beta}{\beta\sqrt{\beta}}(I_x+I_y)+\left(\sqrt{2I_x}+\sqrt{2I_y}\right)=2\sqrt{I_{D3}} \qquad (3.27)$$

If both sides are squared and the higher order terms are ignored, the drain current of M3 is given by:

$$I_{D3}=\sqrt{I_xI_y}+\frac{I_x+I_y}{2}+\frac{\Delta\beta\theta}{\beta\sqrt{\beta}}(I_x+I_y)\left(\sqrt{2I_x}+\sqrt{2I_y}\right) \qquad (3.28)$$

The second term to the right of equation (3.28) is subtracted using transistors M13 and M14 and the output current is given by:

$$I'_{out} = \sqrt{I_x I_y} + \frac{\Delta\beta\theta}{\beta\sqrt{\beta}}\left(I_x + I_y\right)\left(\sqrt{2I_x} + \sqrt{2I_y}\right) \tag{3.29}$$

which results in an absolute error given by:

$$I_{error} = \left|\frac{\Delta\beta\theta}{\beta\sqrt{\beta}}\left(I_x + I_y\right)\left(\sqrt{2I_x} + \sqrt{2I_y}\right)\right| \tag{3.30}$$

The current error quantity in equation (2.30) can be calculated such as: $I_x=80\mu A$, $I_y=3\mu A$, $\theta=0.25V^{-1}$, $\beta=86\mu A/V^2$ and $(\Delta\beta=1\%\ of\ \beta)\ =0.86\mu A/V^2$, then the maximum error is 0.337µA which corresponds to a relative error of 2.2%. This error appears that the proposed circuit has acceptable range with the transconductance parameter mismatch.

3.2.3.3 Threshold Voltage Mismatch

As mentioned before, the threshold voltage (V_{TH}) depends on the source-bulk potential (V_{SB}) as expressed in equation (1.3). With reference to the proposed square-rooting circuit shown in Figure (3.1), we can see that the bulk of all transistors except M2 and M4 are connected to the source, hence the source-bulk voltage (V_{SB}) will be zero. Thus, these transistors will have zero-bias threshold voltage and $V_{TH}=V_{THO}$. However in n-well technology, to avoid the body effect of PMOS transistors M2 and M4, the cascaded MOS transistor are placed in a separate wells to make $V_{SB}=0$ and hence $V_{TH}=V_{THO}$.

If it is assumed that the threshold mismatch is distributed across both transistors M1 and M4 such that:

$$V_{TH1} = V_{TH} + \Delta V_{TH} \tag{3.31}$$

$$V_{TH4} = V_{TH} - \Delta V_{TH} \tag{3.32}$$

where V_{TH} is the threshold value of M1 and M4 and ΔV_{TH} is the mismatch term, then the gate-source voltage of these transistors can be expressed as:

$$V_{GS1} \approx \frac{I_{D1}\theta_1}{\beta_1} + \sqrt{\frac{2I_{D1}}{\beta_1}} + \left(V_{TH} + \Delta V_{TH}\right) \tag{3.33}$$

$$V_{GS4} \approx \frac{I_{D4}\theta_4}{\beta_4} + \sqrt{\frac{2I_{D4}}{\beta_4}} + \left(V_{TH} - \Delta V_{TH}\right) \tag{3.34}$$

Combining equations (3.1), (3.33) and (3.34) yield:

$$\Delta V_{TH} + \frac{I_{D1}\theta_1}{\beta_1} + \sqrt{\frac{2I_{D1}}{\beta_1}} + \frac{I_{D2}\theta_2}{\beta_2} + \sqrt{\frac{2I_{D2}}{\beta_2}} = \frac{I_{D3}\theta_3}{\beta_2} + \sqrt{\frac{2I_{D3}}{\beta_3}} + \frac{I_{D4}\theta_4}{\beta_4} + \sqrt{\frac{2I_{D4}}{\beta_4}} - \Delta V_{TH} \tag{3.35}$$

Following the same analysis as before, it is easy to show that:

$$\Delta V_{TH} + \sqrt{\frac{2I_x}{\beta}} + \sqrt{\frac{2I_y}{\beta}} = 2\sqrt{\frac{I_{D3}}{\beta}} - \Delta V_{TH} \tag{3.36}$$

If both sides are squared and the higher order terms are ignored, the drain current of M3 is given by:

$$I_{D3} = \sqrt{I_x I_y} + \frac{I_x + I_y}{2} + \Delta V_{TH}\sqrt{2\beta I_x} + \Delta V_{TH}\sqrt{2\beta I_y} \tag{3.37}$$

The second term to the right of equation (3.37) is subtracted and the output current is given by:

$$I'_{out} = \sqrt{I_x I_y} + \Delta V_{TH}\sqrt{2\beta I_x} + \Delta V_{TH}\sqrt{2\beta I_y} \tag{3.38}$$

which results in an absolute error given by:

$$I_{error} = \left| I_{out} - I'_{out} \right| = \left| \Delta V_{TH} \sqrt{2\beta} \left(\sqrt{I_x} + \sqrt{I_y} \right) \right| \tag{3.39}$$

To calculate the error due to threshold voltage mismatch using equation (3.23), consider the worst case where $Ix=80\mu A$, $I_y=3\mu A$, $\beta=86\mu A/V^2$, $L=0.35\mu m$ and $\Delta V_{TH} = \frac{0.1 \times t_{ox}}{\sqrt{W \times L}} = \frac{0.1 \times 4.1 \times 10^{-9}}{\sqrt{5 \times 10^{-6} \times 0.35 \times 10^{-6}}} = 0.309mV$, then the maximum error is 43.3nA which corresponds to a relative error of 0.3%.

Again, with reference to Figure (3.1), the drain currents of M10 and M11 are forced to be equal to the drain current of M3 and hence the effect of carrier mobility reduction in MTL loop can be canceled. So, study of threshold mismatch in transistors M10 and M11 is critical in determining the accuracy of the proposed circuit. Considering this mismatch, the gate-source voltage of transistors M10 and M11 is given by:

$$V_{GS10} = \sqrt{\frac{2I_{D10}}{\beta}} + V_{TH} + \Delta V_{TH} \tag{3.40}$$

$$V_{GS11} = \sqrt{\frac{2I_{D11}}{\beta}} + V_{TH} + \Delta V_{TH} \tag{3.41}$$

For M8, the gate-source voltage can be written as:

$$V_{GS8} = \sqrt{\frac{2I_x}{\beta}} + V_{TH} \tag{3.42}$$

With reference to Figure (3.1), noting $V_{GS8} = V_{GS10}$, then:

$$\sqrt{\frac{2I_x}{\beta}} + V_{TH} = \sqrt{\frac{2I_{D10}}{\beta}} + V_{TH} + \Delta V_{TH} \tag{3.43}$$

Equation (3.43) can be rewritten as:

$$\sqrt{\frac{2I_{D10}}{\beta}} = \sqrt{\frac{2I_x}{\beta}} - \Delta V_{TH} \tag{3.44}$$

Squaring both sides and ignoring term of ΔV_{TH} containing higher orders, the drain current of M10 is given by:

$$I_{D10} = I_x - \Delta V_{TH}\sqrt{2\beta \times I_x} \tag{3.45}$$

Also for M12, the gate-source voltage can be written as:

$$V_{GS12} = \sqrt{\frac{2I_y}{\beta}} + V_{TH} \tag{3.46}$$

Noting $V_{GS11} = V_{GS12}$, then I_{D11} becomes:

$$I_{D11} = I_y - \Delta V_{TH}\sqrt{2\beta \times I_y} \tag{3.47}$$

Again, with reference to Figure (3.1), the drain current of M3 is given by:

$$I_{D3} = I_{D10} + I_{D11} \tag{3.48}$$

Substituting equations (3.45) and (3.47) into equation (3.48) to get:

$$I_{D3} = I_x + I_y - \Delta V_{TH}\sqrt{\beta}\left(\sqrt{2I_x} + \sqrt{2I_y}\right) \tag{3.49}$$

Combining equations (3.6) and (3.49) to get:

$$\sqrt{2I_x} + \sqrt{2I_y} + \theta\Delta V_{TH}\left(\sqrt{2I_x} + \sqrt{2I_y}\right) = 2\sqrt{I_{D3}} \tag{3.50}$$

Squaring both sides of equation (3.50) and ignoring higher order terms, the drain current of M3 is given by:

$$I_{D3} = \sqrt{I_x I_y} + \frac{I_x + I_y}{2} + \theta \Delta V_{TH}\left(I_x + I_y\right) + 2\theta \Delta V_{TH}\sqrt{I_x I_y} \qquad (3.51)$$

The second term to the right of equation (3.51) is subtracted and the output current is given by:

$$I'_{out} = \sqrt{I_x I_y} + \theta \Delta V_{TH}\left(I_x + I_y\right) + 2\theta \Delta V_{TH}\sqrt{I_x I_y} \qquad (3.52)$$

which results in an absolute error as:

$$I_{error} = \left|I_{out} - I'_{out}\right| = \left|\theta \Delta V_{TH}\left(I_x + I_y\right) + 2\theta \Delta V_{TH}\sqrt{I_x I_y}\right| \qquad (3.53)$$

As an example, if I_x=*80μA*, I_y=*3μA*, θ=*0.25V*$^{-1}$ and $\Delta V_{TH} = 0.309mV$, the maximum error is *8.8nA* which corresponds to a relative error of *0.06%*.

From above analysis, we can say that the output current of the proposed circuit has very good performance with the threshold voltage mismatch.

Simulation Result of the Threshold Voltage Mismatch

In short-channel MOSFET models, the effect of V_{TH} variation cannot be modeled easily in T-Spice. The definition of a Gaussian distribution for V_{TH0} depends on the exact dimensions of each MOS transistor as stated in table (3.2). Hence, for modeling the impact of V_{TH} variation in MOSFET, a DC voltage source device is added in series with the gate terminal of the device which has a Gaussian distribution with zero mean value as shown in Figure (3.7).

Table 3.2 Transistor Standard deviation of MOS parameters

	NMOS	PMOS
$\Delta V_{TH}(mV)$	$\frac{0.1\times t_{ox(NMOS)}}{\sqrt{W\times L}}$	$\frac{0.1\times t_{ox(PMOS)}}{\sqrt{W\times L}}$

where ΔV_{TH} is the threshold variation, t_{ox} is the gate oxide thickness, W and L are the dimension of the transistor.

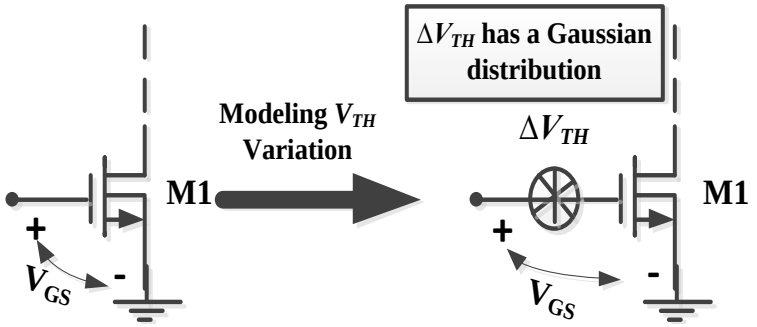

Figure 3.7 Modeling V_{TH} variations using a DC voltage source with Gaussian distribution

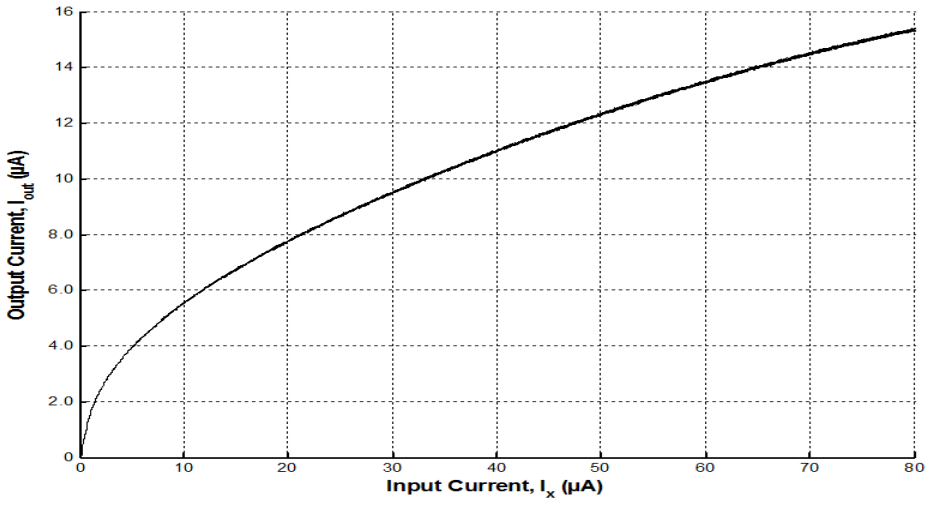

Figure 3.8 Monte Carlo analysis with Gaussian distribution for threshold variation

Simulating threshold mismatch for the proposed square-rooting circuit using the above method was carried out using Monte Carlo analysis. After 100 times iterations (Monte=100), the simulation result of threshold mismatch for the transistors M1 and M4 shown in Figure (3.8) indicates that the corresponding maximum deviation of the output current is about 1.2%. This means the proposed circuit is almost insensitive to threshold voltage mismatch.

3.2.3.4 Channel Length Mismatch

The same analysis can be performed on mismatch in channel length parameter *L*. If it is assumed that transistors M1 and M4 have channel length mismatch such that:

$$L_1 = L + \Delta L \tag{3.54}$$

$$L_4 = L - \Delta L \tag{3.55}$$

where L is the channel length value of M1 and M4 and ΔL is the mismatch term, then the gate-source potential of these transistors can be expressed as:

$$V_{GS1} \approx \frac{I_{D1}\theta_1\left(\frac{L+\Delta L}{L}\right)}{\beta_1} + \sqrt{\frac{2I_{D1}\left(\frac{L+\Delta L}{L}\right)}{\beta_1}} + V_{TH} \tag{3.56}$$

$$V_{GS4} \approx \frac{I_{D4}\theta_4\left(\frac{L-\Delta L}{L}\right)}{\beta_4} + \sqrt{\frac{2I_{D4}\left(\frac{L-\Delta L}{L}\right)}{\beta_4}} + V_{TH} \tag{3.57}$$

where $\beta_i = k'_{pi}\frac{W}{L}$ is transconductance parameter for the transistor M_i;

Combining equations (3.1), (3.56) and (3.57) yield:

$$\frac{I_{D1}\theta_1\left(\frac{L+\Delta L}{L}\right)}{\beta_1}+\sqrt{\frac{2I_{D1}\left(\frac{L+\Delta L}{L}\right)}{\beta_1}}+\frac{I_{D2}\theta_2}{\beta_2}+\sqrt{\frac{2I_{D2}}{\beta_2}}=\frac{I_{D3}\theta_3}{\beta_3}+\sqrt{\frac{2I_{D3}}{\beta_3}}+\frac{I_{D4}\theta_4\left(\frac{L-\Delta L}{L}\right)}{\beta_4}+\sqrt{\frac{2I_{D4}\left(\frac{L-\Delta L}{L}\right)}{\beta_4}} \quad (3.58)$$

Following the same analysis as before, it is easy to show that:

$$\left(\frac{3\theta\Delta L}{2L\sqrt{\beta}}I_x+\frac{\theta\Delta L}{2L\sqrt{\beta}}I_y\right)+\left(\sqrt{2I_x\left(\frac{L+\Delta L}{L}\right)}+\sqrt{2I_y}\right)=\left(\sqrt{2I_{D3}}+\sqrt{2I_{D3}\left(\frac{L-\Delta L}{L}\right)}\right) \quad (3.59)$$

If both sides are squared and the higher order terms are ignored, the drain current of M3 is given by:

$$2I_{D3}\left(\left(1+\frac{\Delta L}{L}\right)+\sqrt{\left(1+\frac{\Delta L}{L}\right)}\right)=2I_x\left(1+\frac{\Delta L}{L}\right)+2I_y+4\sqrt{2I_xI_y\left(1+\frac{\Delta L}{L}\right)}+\left\{\begin{array}{l}\frac{3\theta\Delta L}{L\sqrt{\beta}}I_x\left(\sqrt{2I_x\left(1+\frac{\Delta L}{L}\right)}+\sqrt{2I_y}\right)\\+\frac{\theta\Delta L}{L\sqrt{\beta}}I_y\left(\sqrt{2I_x\left(1+\frac{\Delta L}{L}\right)}+\sqrt{2I_y}\right)\end{array}\right\} \quad (3.60)$$

But$\left(\frac{\Delta L}{L}<<1\right)$, then:

$$I_{D3}=\sqrt{I_xI_y}+\frac{I_x+I_y}{2}+\frac{3\theta\Delta L}{4L\sqrt{\beta}}I_x\left(\sqrt{2I_x}+\sqrt{2I_y}\right)+\frac{\theta\Delta L}{4L\sqrt{\beta}}I_y\left(\sqrt{2I_x}+\sqrt{2I_y}\right) \quad (3.61)$$

The second term to the right of equation (3.61) is subtracted and the output current can be written as:

$$I'_{out}=\sqrt{2I_xI_y}+\frac{3\theta\Delta L}{4L\sqrt{\beta}}I_x\left(\sqrt{2I_x}+\sqrt{2I_y}\right)+\frac{\theta\Delta L}{4L\sqrt{\beta}}I_y\left(\sqrt{2I_x}+\sqrt{2I_y}\right) \quad (3.62)$$

which results in an absolute error given by:

$$I_{error}=\left|\frac{3\theta\Delta L}{4L\sqrt{\beta}}I_x\left(\sqrt{2I_x}+\sqrt{2I_y}\right)+\frac{\theta\Delta L}{4L\sqrt{\beta}}I_y\left(\sqrt{2I_x}+\sqrt{2I_y}\right)\right| \quad (3.63)$$

To calculate the error in equation (3.63), we consider I_x=*80μA*, I_y=*3μA*, θ=*0.25V*$^{-1}$, β=*86μA/V*^{2}, *L=0.35μm* and $\Delta L = 0.007\mu m$, then the maximum error is *0.488μA* which is equivalent to *3%*.

Study of channel length mismatch in transistors M10 and M11 is also critical in determining the accuracy of the proposed circuit. Considering this mismatch, the gate-source voltage of transistors M10 and M11 is given by:

$$V_{GS10} = \sqrt{\frac{2I_{D10}\left(\frac{L+\Delta L}{L}\right)}{\beta}} + V_{TH} \tag{3.64}$$

$$V_{GS11} = \sqrt{\frac{2I_{D11}\left(\frac{L+\Delta L}{L}\right)}{\beta}} + V_{TH} \tag{3.65}$$

Where, β is defined before.

With reference to Figure (3.1), noting V_{GS8}= V_{GS10}, then substituting equations (3.42) and (3.64) to get:

$$\sqrt{\frac{2I_x}{\beta}} + V_{TH} = \sqrt{\frac{2I_{D10}\left(\frac{L+\Delta L}{L}\right)}{\beta}} + V_{TH} \tag{3.66}$$

Since the drain current is in μA, then the drain current of M10 is given by:

$$I_{D10} = \frac{I_x}{\left(\frac{L+\Delta L}{L}\right)} = I_x\left(\frac{1}{1+\frac{\Delta L}{L}}\right) \tag{3.67}$$

But $\left(\frac{\Delta L}{L} << 1\right)$, then:

$$I_{D10} = I_x\left(\frac{1}{1+\frac{\Delta L}{L}}\right) \approx I_x\left(1-\frac{\Delta L}{L}\right) \approx I_x - \frac{\Delta L}{L} I_x \tag{3.68}$$

With reference to Figure (3.1), noting $V_{GS11} = V_{GS12}$, and substituting equations (3.46) and (3.65), the drain current of M11 is given as:

$$I_{D11} = I_y - \frac{\Delta L}{L} I_y \tag{3.69}$$

Combining equations (3.48), (3.68) and (3.69) to get:

$$I_{D3} = I_x + I_y - \frac{\Delta L}{L}\left(I_x + I_y\right) \tag{3.70}$$

Combining equations (3.6) and (3.70) to get:

$$\left(\sqrt{2I_x} + \sqrt{2I_y}\right) + \frac{\theta \Delta L}{L\sqrt{\beta}}\left(I_x + I_y\right) = 2\sqrt{I_{D3}} \tag{3.71}$$

Squaring both sides and ignoring higher order terms, the drain current of M3 can be expressed as:

$$I_{D3} = \sqrt{I_x I_y} + \frac{I_x + I_y}{2} + \frac{\theta \Delta L}{2L\sqrt{\beta}}\left(I_x + I_y\right)\left(\sqrt{2I_x} + \sqrt{2I_y}\right) \tag{3.72}$$

The second term to the right of equation (3.58) is subtracted and the output current is given by:

$$I'_{out} = \sqrt{I_x I_y} + \frac{\theta \Delta L}{2L\sqrt{\beta}}\left(I_x + I_y\right)\left(\sqrt{2I_x} + \sqrt{2I_y}\right) \tag{3.73}$$

which results in an absolute error given by:

$$I_{error} = |I_{out} - I'_{out}| = \left| \frac{\theta \Delta L}{2L\sqrt{\beta}} (I_x + I_y)\left(\sqrt{2I_x} + \sqrt{2I_y}\right) \right| \qquad (3.74)$$

As an example, if I_x=80μA, I_y=3μA, θ=0.25V^{-1}, β=86μA/V^2, L=0.35μm and $\Delta L = 0.007 \mu m$, the maximum error is 0.337μA which is equivalent to 2.2%. This means the proposed design has acceptable range with channel length mismatch.

In general, circuits designed using short channel MOSFETs are sensitive to produce variation especially, channel length variation. Some layout techniques are usually used to minimize this effect.

Simulation Result of the Channel Length Mismatch

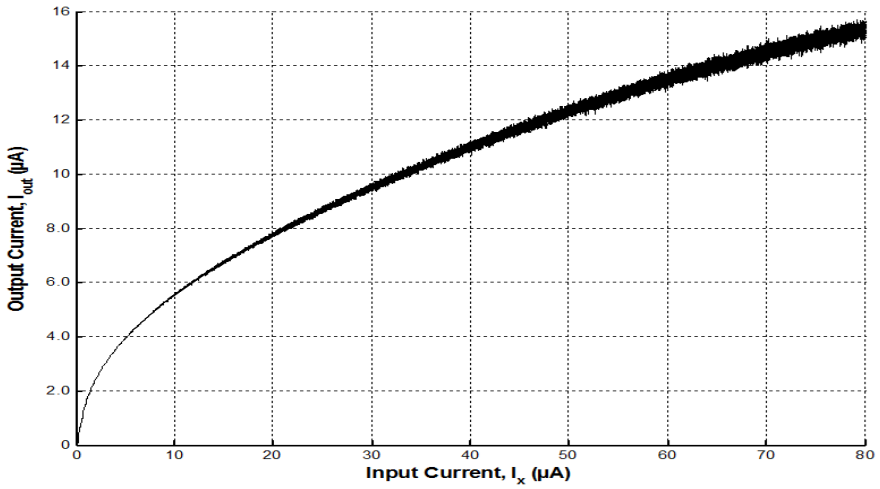

Figure 3.9 Monte Carlo analysis with Gaussian distribution for 2% channel length variation

Simulation for channel length mismatch was carried out for transistors M1 and M4 in MTL as it is the most important block. Mont Carlo analysis was carried out for 100 times (Monte=100) with mean value of 0.35μm and three sigma variation of (3*0.02*0.35μ) =0.021μm. The simulation result for 2% channel length mismatch of the transistors M1

and M4 shown in Figure (3.9) indicates that the corresponding maximum deviation of the output current is about 3%. This means the proposed circuit is a little sensitive to channel length mismatch.

3.2.3.5 Matching Currents in the Mirror

With reference to the proposed square-rooting circuit shown in Figure (3.1), we can see that the circuit depends on basic current mirrors; therefor the accuracy of the proposed circuit is directly related to the accuracy of current mirrors. It is well known that, the threshold voltage and channel length are critical in determining the overall accuracy of the current mirror. In this section, the mismatch of threshold voltage and channel length of transistors in current mirror will be analyzed.

- **Threshold Voltage Mismatch**

To examine the effect of threshold mismatch in the current mirror, let's assume that the threshold mismatch is distributed across transistors M8 and M9 such that:

$$V_{TH8} = V_{TH} - \Delta V_{TH} \tag{3.75}$$

$$V_{TH9} = V_{TH} + \Delta V_{TH} \tag{3.76}$$

Where V_{TH} is the threshold value of M8 and M9 and ΔV_{TH} is the mismatch term, then the gate-source voltage of these transistors can be written as:

$$V_{GS8} = \sqrt{\frac{2I_x}{\beta}} + \left(V_{TH} - \Delta V_{TH}\right) \tag{3.77}$$

$$V_{GS9} = \sqrt{\frac{2I_{D9}}{\beta}} + \left(V_{TH} + \Delta V_{TH}\right) \tag{3.78}$$

Since M8 and M9 have the same value for V_{GS}, then:

$$\sqrt{\frac{2I_x}{\beta}} + \left(V_{TH} - \Delta V_{TH}\right) = \sqrt{\frac{2I_{D9}}{\beta}} + \left(V_{TH} + \Delta V_{TH}\right) \tag{3.79}$$

Equation (3.79) can be rewritten as:

$$\sqrt{\frac{2I_{D9}}{\beta}} = \left(\sqrt{\frac{2I_x}{\beta}} - 2\Delta V_{TH}\right) \tag{3.80}$$

If both sides of the equation (3.80) are squared and the higher order terms are ignored, the relation between I_{D9} and I_x is given by:

$$\frac{I_{D9}}{I_x} = 1 - \frac{4\Delta V_{TH}}{[V_{GS} - V_{TH} + \Delta V_{TH}]} \approx 1 - \frac{4\Delta V_{TH}}{[V_{GS} - V_{TH}]} \approx 1 - \frac{4\Delta V_{TH}}{V_{ov}} \tag{3.81}$$

where V_{ov} is the overdrive voltage:

Equation (3.81) shows that as V_{GS} decreases, the error in the mirrored currents increases due to threshold voltage mismatch. However, to reduce the effects of threshold voltage mismatch, a large overdrive voltage should be used.

- **Channel Length Mismatch**

The same analysis can be performed on the channel length parameter L, if $L_8=L-\Delta L$ and $L_9=L+\Delta L$, where L is the channel length value of M8 and M9 and ΔL is the mismatch term, then:

$$V_{GS8} = \sqrt{\frac{2I_x}{k'_p \frac{W}{L-\Delta L}}} + V_{TH} \tag{3.82}$$

$$V_{GS9} = \sqrt{\frac{2I_{D9}}{k'_p \frac{W}{L+\Delta L}}} + V_{TH} \tag{3.83}$$

Since M8 and M9 have the same value for V_{GS}, then:

$$\sqrt{\frac{2I_x}{k'_p \frac{W}{L-\Delta L}}} + V_{TH} = \sqrt{\frac{2I_{D9}}{k'_p \frac{W}{L+\Delta L}}} + V_{TH} \tag{3.84}$$

Since $\left(\frac{\Delta L}{L} << 1\right)$, the difference in the currents becomes:

$$\frac{I_{D9}}{I_x} = \frac{k'_p \frac{W}{L+\Delta L}}{k'_p \frac{W}{L-\Delta L}} = \frac{L-\Delta L}{L+\Delta L} \approx 1 - \frac{2\Delta L}{L} \tag{3.85}$$

Equation (3.85) confirms that as L decreases, the error in the mirrored currents increases due to channel length mismatch. However, to reduce this mismatch, a long-channel should be used.

Table (3.3) summarizes the comparison of the performance between the proposed square-rooting circuit and recently published works. It is clear from the table; the proposed circuit has a better performance than prior art in terms of input range, bandwidth and silicon area. However, the proposed circuit is simulated using 0.18µm CMOS technology and it is used transistors with short channel-length (L=0.35µm) in comparison with previously reported square-rooters shown in table (3.3) which used long channel- length transistors to reduce/cancel the error caused by carrier mobility reduction and channel length modulation to improve the accuracy of the designed circuits.

Table 3.3 Comparison table between different square-rooting circuits

Ref.	Public Year	Type (In/Out)	Tech. (µA)	Minim. L (µm)	Supply Voltage (V)	Input Range (µA)	Power Cons. (µW)	Relative Error (%)	-3 dB Frequency (MHz)	Area (μm^2)
[48]	2009	CI/CO	0.35	0.7	3.0	-	-	-	-	-
[49]	2009	CI/CO	0.18	-	1.5	40	-	-	-	-
[50]	2010	CI/VO	0.25	1.0	±0.7	50	1.4	0.55	-	-
[51]	2007	VI/CO	0.25	1.2	1.8	-	145	2.5	158	410
[52]	2007	CI/CO	0.35	0.7	3.0	10	-	1.26	-	-
This Work	**2013**	**CI/CO**	**0.18**	**0.35**	**2V**	**80**	**22.5**	**0.8**	**216**	**141**

3.3 Current-mode Squaring Circuit

In this section, the proposed current-mode squaring circuit will be introduced. Simulation results and mismatch analysis will be carried out. Finally, summary of performance comparison will be given.

3.3.1 Proposed Current-mode Squaring Circuit

The proposed squaring circuit that is reduced short-channel effect caused by carrier mobility reduction is shown in Figure (3.10). The conventional current-mode squaring circuit which is given in Figure (2.9) is modified as shown in Figure (3.10). The current rectifier circuit is used the cascaded mirror to cancel the channel length modulation effect. The proposed circuit is based on translinear loop formed by transistors (M1-M4). The current I_B is the bias current and I_x is the input current. It will be shown that the output current is given by: $I_{out} = \frac{I_x^{\,2}}{8I_B}$

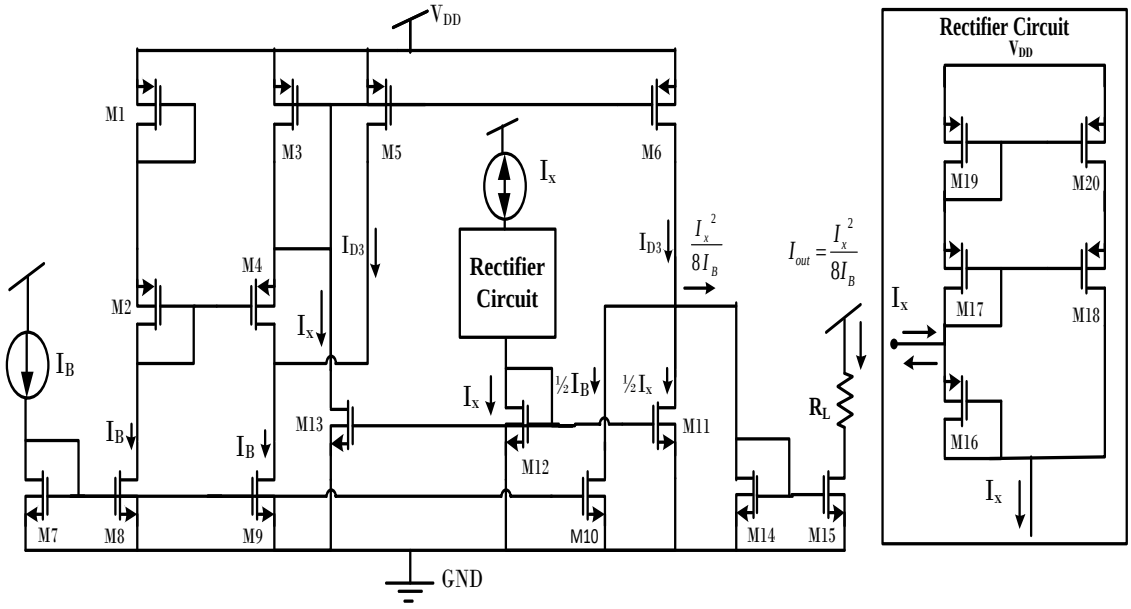

Figure 3.10 Proposed current-mode squaring circuit

With reference to Figure (3.10), writing MTL around transistors M1- M4 to get:

$$V_{SG1} + V_{SG2} = V_{SG3} + V_{SG4} \tag{3.86}$$

If the carrier mobility reduction is taken into consideration, the MOS drain current is given by:

$$I_D = \frac{\beta}{2} \frac{(V_{GS} - V_{TH})^2}{1 + \theta(V_{GS} - V_{TH})} \tag{3.87}$$

where, θ is a fitting parameter and β is the transconductance parameter. Using equation (3.87), the gate-source voltage can be written as:

$$V_{GS} \approx \frac{I_D \theta}{\beta} + \sqrt{\frac{2I_D}{\beta}} + V_{TH} \tag{3.88}$$

Combining equations (3.86) and (3. 88) to get:

$$\frac{I_{D1}\theta_1}{\beta_1}+\sqrt{\frac{2I_{D1}}{\beta_1}}+\frac{I_{D2}\theta_2}{\beta_2}+\sqrt{\frac{2I_{D2}}{\beta_2}}=\frac{I_{D3}\theta_3}{\beta_3}+\sqrt{\frac{2I_{D3}}{\beta_3}}+\frac{I_{D4}\theta_4}{\beta_4}+\sqrt{\frac{2I_{D4}}{\beta_4}} \qquad (3.89)$$

Assuming the aspect ratios of the transistors in MTL satisfy the condition $\beta_1 = \beta_2 = 2\beta$, $\beta_3 = \beta_4 = \beta$ and $\theta_1 = \theta_2 = \theta_3 = \theta_4 = \theta$ where β is the transconductance parameter of the PMOS transistors and θ is a fitting parameter which is equal about $0.25\ V^{-1}$ for 0.18μm process technology.

Equation (3.89) can be rewritten as:

$$\frac{I_{D1}\theta}{2\beta}+\sqrt{\frac{2I_{D1}}{2\beta}}+\frac{I_{D2}\theta}{2\beta}+\sqrt{\frac{2I_{D2}}{2\beta}}=\frac{I_{D3}\theta}{\beta}+\sqrt{\frac{2I_{D3}}{\beta}}+\frac{I_{D4}\theta}{\beta}+\sqrt{\frac{2I_{D4}}{\beta}} \qquad (3.90)$$

With reference to Figure (3.10), the drain current of transistors M1 and M2 are the same, equation (3.90) can be expressed by:

$$\frac{\theta}{\beta}I_B+\frac{2}{\sqrt{\beta}}\sqrt{I_B}=\frac{\theta}{\beta}(I_{D3}+I_{D4})+\frac{1}{\sqrt{\beta}}\left(\sqrt{2I_{D3}}+\sqrt{2I_{D4}}\right) \qquad (3.91)$$

If we force the following condition;

$$\frac{\theta}{\beta}I_B=\frac{\theta}{\beta}(I_{D3}+I_{D4})\ \text{Then:}$$

$$I_B=I_{D3}+I_{D4} \qquad (3.92)$$

Using equations (3.92), then equations (3.91) can be rewritten as:

$$\frac{2}{\sqrt{\beta}}\sqrt{I_B}=\frac{1}{\sqrt{\beta}}\left(\sqrt{2I_{D3}}+\sqrt{2I_{D4}}\right) \qquad (3.93)$$

Equation (3.93) can be rewritten as:

$$\sqrt{2I_{D4}} = 2\sqrt{I_B} - \sqrt{2I_{D3}} \tag{3.94}$$

From the circuit schematic shown in Figure (3.10), with current I_x mirrored in transistor M13, the drain current of M3 is given by:

$$I_{D3} = I_X + I_{D4} \tag{3.95}$$

Combining equations (3.94) and (3.95), the drain current for M4 is given by:

$$I_{D4} = \frac{I_B}{2} - \frac{I_x}{2} + \frac{I_x^{\,2}}{8I_B} \tag{3.96}$$

Combining equations (3.95) and (3.96) to get:

$$I_{D3} = I_X + \frac{I_B}{2} - \frac{I_x}{2} + \frac{I_x^{\,2}}{8I_B} = \frac{I_x}{2} + \frac{I_B}{2} + \frac{I_x^{\,2}}{8I_B} \tag{3.97}$$

The first two terms to the right are subtracted using transistors M10 and M11 and the output current is mirrored via M14 and M15 to get:

$$I_{out} = \frac{I_x^{\,2}}{8I_B} \tag{3.98}$$

Equation (3.98) can be written as:

$$I_{out} = kI_x^2 \tag{3.99}$$

where, $k = \frac{I_B}{8}$

It is clear that equation (3.99) implements squaring circuit with compensation for error due to carrier mobility reduction.

3.3.2 Simulation Results

The functionality of the proposed design is confirmed using Tanner T-spice in 0.18µm CMOS process technology. The bias current I_B is *60 µA* and the input current I_x is swept from *-40* to *40µA*. The circuit is operated from *1.5V* DC supply voltage and the device aspect ratios of all transistors are listed in table (3.4). The output current was measured by forcing it through a load resistor R_L=*10kΩ*.

Table 3.4 Transistor aspect ratios of the squaring circuit

W/L (µm)		W/L (µm)		W/L (µm)		W/L (µm)	
M1	5.0/0.2	M6	2.5/0.2	M11	2.5/0.2	M16	5.0/0.2
M2	5.0/0.2	M7	5.0/0.2	M12	5.0/0.2	M17	5.0/0.2
M3	2.5/0.2	M8	5.0/0.2	M13	5.0/0.2	M18	5.0/0.2
M4	2.5/0.2	M9	5.0/0.2	M14	0.3/0.5	M19	5.0/0.2
M5	2.5/0.2	M10	2.5/0.2	M15	0.3/0.5	M20	5.0/0.2

The DC transfer characteristic of the squaring circuit is shown in Figure (3.11). The figure shows the results for calculated and simulated result for both the conventional and the proposed design. It is clear from the figure that the proposed design is in a close agreement with the theory. Also, Plot of the error between calculated and simulated results is shown in Figure (3.12). The maximum relative error is *1.2%*. The simulated maximum power consumption for the proposed circuit is *326µW*.

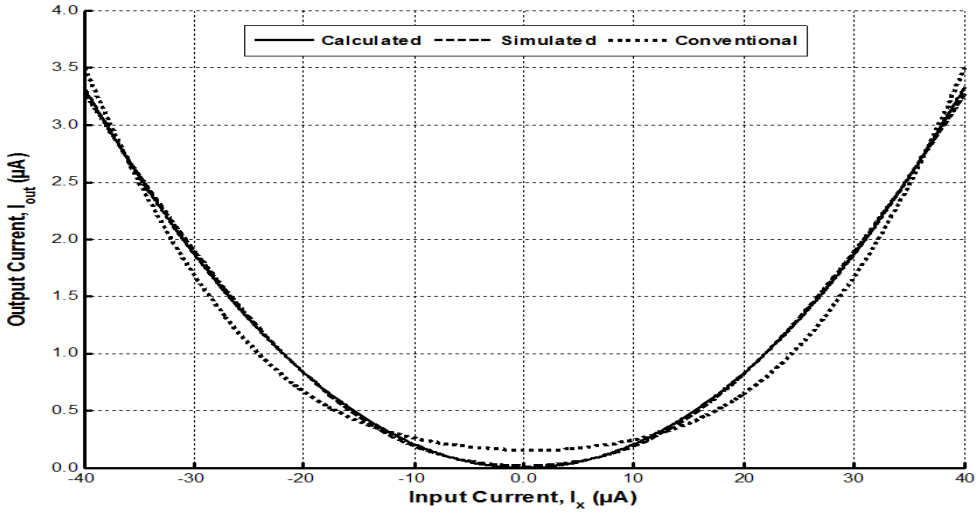

Figure 3.11 The output current of the ideal and the proposed squaring circuit

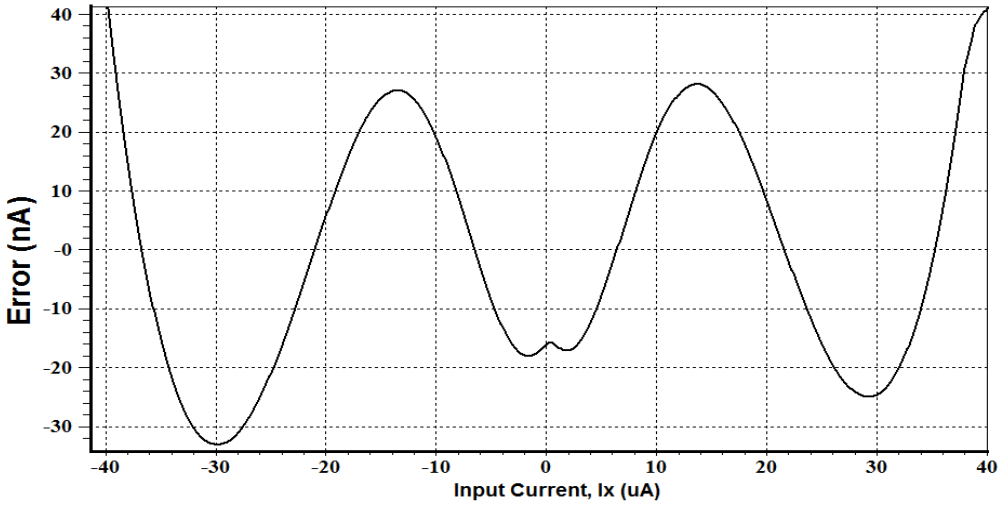

Figure 3.12 Error between calculated and simulated

Simulation for transient analysis was also carried out. The input signal is triangular with *80μA* peak-to-peak and *1MHz* frequency. Figure (3.13) shows input current, the output current and the error between calculated and simulated result.

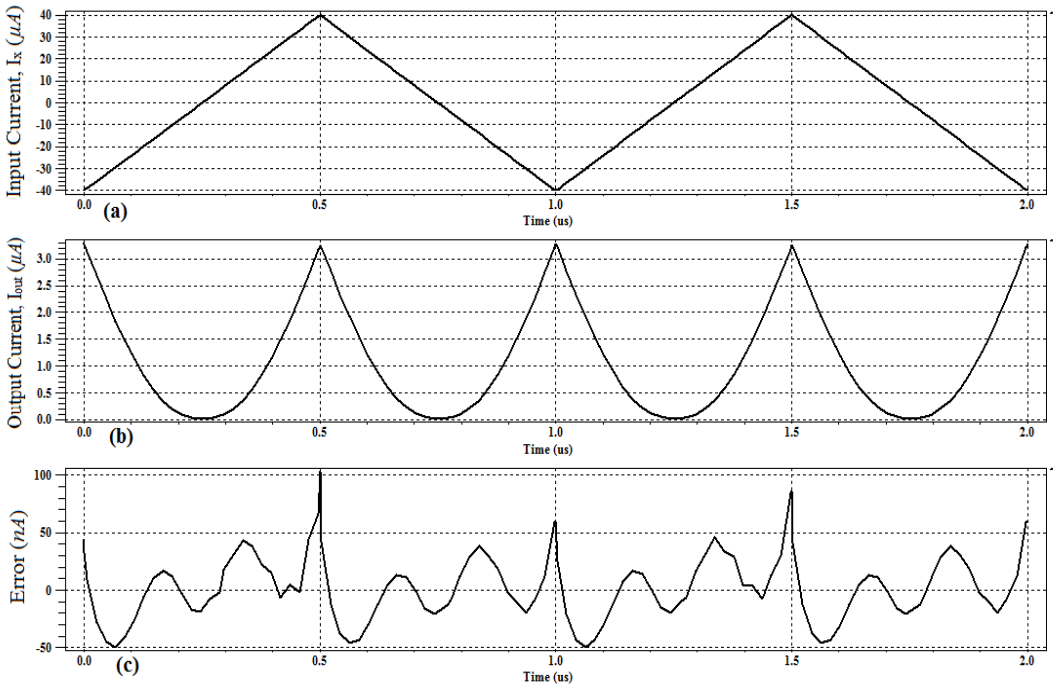

Figure 3.13 Simulation for transient analysis (a) Input signal (b) Output signal (c) Error

Simulation for temperature analysis was carried out. The temperature was swept from -25°C to 75°C in steps of 50°C. The simulation result shown in Figure (3.14) shows that the maximum deviation from the calculated value is 0.68μA (20.4%) which happened at 75°C. This means that the proposed circuit is sensitive with temperature variation.

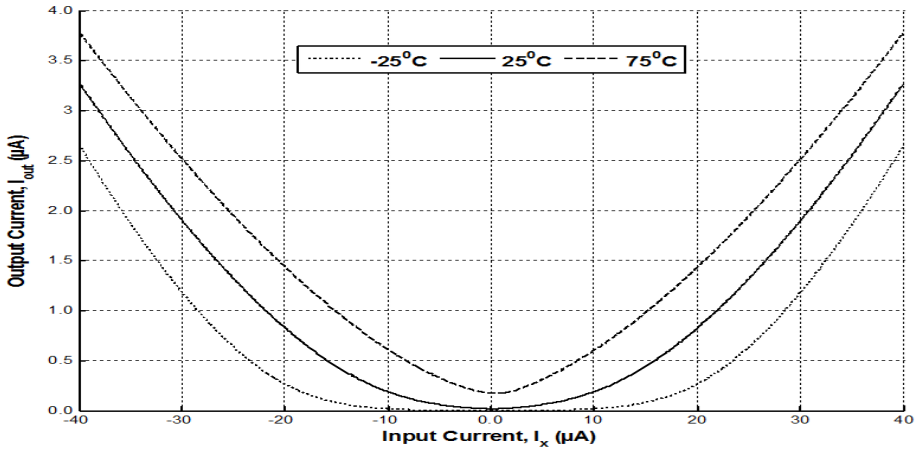

Figure 3.14 Simulation result for temperature variation

The circuit was simulated for the frequency response. The input signal I_x is applied and the frequency is swept from 10Hz to 10GHz. Simulation result shown in Figure (3.15) indicates the upper *3dB* frequency is *340MHz*.

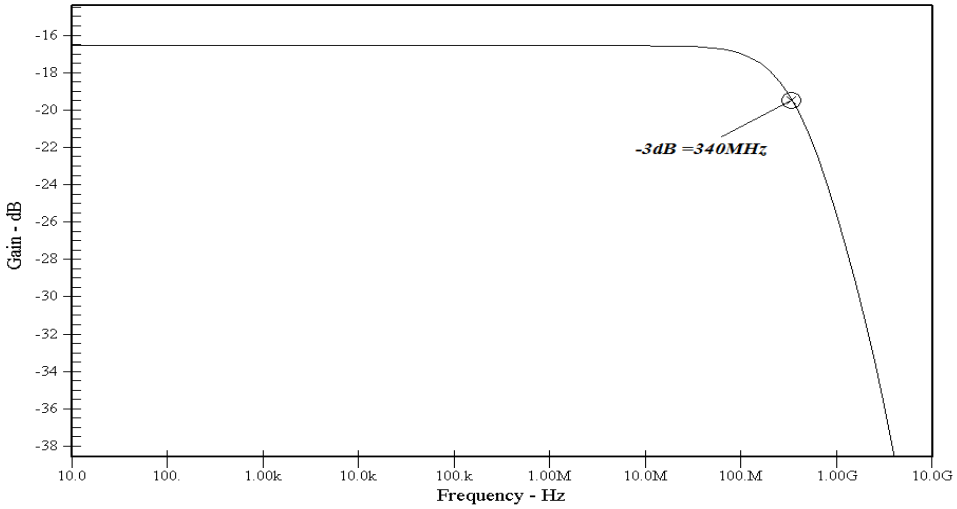

Figure 3.15 Frequency response of the proposed squaring circuit

3.3.3 Mismatch Analysis

The previous analysis was carried out based on the assumption that the mobility parameter, transconductance parameter, threshold voltage and channel length of transistors are matched. In this section, the influence of mismatch of these parameters in the MTL of the proposed circuit will be analyzed.

3.3.3.1 Mobility Parameter Mismatch

If it is assumed that the mobility parameter of transistors M1-M4 of the proposed squaring circuit is not perfectly matched, and assuming all other parameters are matched, then equation (3.91) can be rewritten as:

$$\frac{(\theta+\Delta\theta)}{\beta} I_B + \frac{2}{\sqrt{\beta}}\sqrt{I_B} = \frac{(\theta-\Delta\theta)}{\beta}(I_{D3}+I_{D4}) + \frac{1}{\sqrt{\beta}}\left(\sqrt{2I_{D3}}+\sqrt{2I_{D4}}\right) \tag{3.100}$$

Following the same analysis as before, it is easy to show that:

$$\frac{2\Delta\theta}{\sqrt{\beta}} I_B + 2\sqrt{I_B} = \sqrt{2I_{D3}} + \sqrt{2I_{D4}} \tag{3.101}$$

Substituting equation (3.95) into equation (3.101) and squaring both side twice and ignoring higher order terms, the drain current of M3 is given by:

$$I_{D3} = \frac{I_x^2}{8I_B\left(1+\frac{2\Delta\theta}{\sqrt{\beta}}\sqrt{I_B}\right)} + \frac{I_x\left(1+\frac{2\Delta\theta}{\sqrt{\beta}}\sqrt{I_B}\right)+I_B}{2\left(1+\frac{2\Delta\theta}{\sqrt{\beta}}\sqrt{I_B}\right)} + \frac{\Delta\theta}{\sqrt{\beta}}\frac{\sqrt{I_B}\times(2I_B)}{\left(1+\frac{2\Delta\theta}{\sqrt{\beta}}\sqrt{I_B}\right)} \tag{3.102}$$

But$\left(\frac{2\Delta\theta}{\sqrt{\beta}}\sqrt{I_B} << 1\right)$, equation (3.102) can be rewritten as:

$$I_{D3} = \frac{I_x^2}{8I_B} + \frac{I_x+I_B}{2} + \frac{2\Delta\theta}{\sqrt{\beta}} I_B\sqrt{I_B} \tag{3.103}$$

The second term to the right of equation (3.103) is subtracted using transistors M10 and M11, and the output current is given as:

$$I'_{out} = \frac{I_x^2}{8I_B} + \frac{2\Delta\theta}{\sqrt{\beta}} I_B\sqrt{I_B} \tag{3.104}$$

which results in an absolute error given by:

$$I_{error} = |I_{out} - I'_{out}| = \left|\frac{2\Delta\theta}{\sqrt{\beta}} I_B\sqrt{I_B}\right| \tag{3.105}$$

To evaluate the error due to mobility parameter mismatch using equation (3.105), consider the worst case where I_B=60μA, β=86μA/V^2, θ=0.25V^{-1} and ($\Delta\theta$=1% of θ)

$=0.0025\ V^{-1}$, then the maximum error is 0.25μA which corresponds to a relative error of 7.5%. It is clear that the mismatch in carrier mobility parameter will degrade the accuracy of the circuit designed using MTL approach and maybe other approach.

3.3.3.2 Transconductance Parameter Mismatch

The same analysis can be performed on the transconductance parameter value of transistors M1-M4 of the proposed squaring circuit and the equation (3.91) can be rewritten as:

$$\frac{\theta}{(\beta-\Delta\beta)}I_B+\frac{2}{\sqrt{(\beta-\Delta\beta)}}\sqrt{I_B}=\frac{\theta}{(\beta+\Delta\beta)}(I_{D3}+I_{D4})+\frac{1}{\sqrt{(\beta+\Delta\beta)}}\left(\sqrt{2I_{D3}}+\sqrt{2I_{D4}}\right) \tag{3.106}$$

Following the same analysis as before, it is easy to show that:

$$\left\{\begin{array}{l}\dfrac{\theta}{\beta}\left(\dfrac{1}{1-\dfrac{\Delta\beta}{\beta}}\right)I_B-\dfrac{\theta}{\beta}\left(\dfrac{1}{1+\dfrac{\Delta\beta}{\beta}}\right)I_B \\ +\dfrac{2}{\sqrt{\beta}}\left(\sqrt{\dfrac{1}{1-\dfrac{\Delta\beta}{\beta}}}\right)I_B\end{array}\right\}=\frac{1}{\sqrt{\beta}}\left(\sqrt{\frac{1}{1+\frac{\Delta\beta}{\beta}}}\right)\left(\sqrt{I_{D3}}+\sqrt{I_{D4}}\right) \tag{3.107}$$

It is well known that $\left(\dfrac{1}{1\pm x}\approx 1\mp x\right)$ if $(x<<1)$. Using this approximation in equation (3.107) to get

$$\left\{\begin{array}{l}\dfrac{\theta}{\beta}\left(1+\dfrac{\Delta\beta}{\beta}\right)(I_x+I_y)-\dfrac{\theta}{\beta}\left(1-\dfrac{\Delta\beta}{\beta}\right)(I_x+I_y)+ \\ \dfrac{1}{\sqrt{\beta}}\left(\sqrt{\left(1+\dfrac{\Delta\beta}{\beta}\right)}\right)\left(\sqrt{2I_x}+\sqrt{2I_y}\right)\end{array}\right\}=\frac{2}{\sqrt{\beta}}\left(\sqrt{\left(1-\frac{\Delta\beta}{\beta}\right)}\right)\sqrt{I_{D3}} \tag{3.108}$$

But $\left(\dfrac{\Delta\beta}{\beta}<<1\right)$, then equation (3.108) can be rewritten as:

$$\frac{2\theta\Delta\beta}{\beta\sqrt{\beta}} I_B + 2\sqrt{I_B} = 2\sqrt{I_{D3}} + 2\sqrt{I_{D4}} \tag{3.109}$$

Substituting equation (3.95) into equation (3.109) and squaring both side twice and ignoring higher order terms, the drain current of M3 is given by:

$$I_{D3} = \frac{I_x^2}{8I_B\left(1+\frac{2\theta\Delta\beta}{\beta\sqrt{\beta}}\sqrt{I_B}\right)} + \frac{I_x\left(1+\frac{2\theta\Delta\beta}{\beta\sqrt{\beta}}\sqrt{I_B}\right)+I_B}{2\left(1+\frac{2\theta\Delta\beta}{\beta\sqrt{\beta}}\sqrt{I_B}\right)} + \frac{\theta\Delta\beta}{\beta\sqrt{\beta}}\frac{\sqrt{I_B}(2I_B)}{\left(1+\frac{2\theta\Delta\beta}{\beta\sqrt{\beta}}\sqrt{I_B}\right)} \tag{3.110}$$

But $\left(\frac{2\theta\Delta\beta}{\beta\sqrt{\beta}}\sqrt{I_B} << 1\right)$, equation (3.110) can be rewritten as:

$$I_{D3} = \frac{I_x^2}{8I_B} + \frac{I_x + I_B}{2} + \frac{\theta\Delta\beta}{\beta\sqrt{\beta}}\sqrt{I_B}(2I_B) \tag{3.111}$$

The second term to the right of equation (3.111) is subtracted using M10 and M11, and the output current is given as:

$$I'_{out} = \frac{I_x^2}{8I_B} + \frac{2\theta\Delta\beta}{\beta\sqrt{\beta}} I_B\sqrt{I_B} \tag{3.112}$$

which results in an absolute error given by:

$$I_{error} = |I_{out} - I'_{out}| = \left|\frac{2\theta\Delta\beta}{\beta\sqrt{\beta}} I_B\sqrt{I_B}\right| \tag{3.113}$$

To evaluate the error due to the transconductance parameter mismatch using equation (3.113), we consider I_B=60μA, θ=0.25V^{-1}, β=86μA/V^2 and ($\Delta\beta$=1% of β) =0.86μA/V^2, then the maximum error is 0.25μA which is equivalent to a relative error of 7.5%. This means that the proposed circuit is also very sensitive to mismatch in the transconductance parameter.

3.3.3.3 Threshold Voltage Mismatch

As stated before, the threshold voltage V_{TH} increases as the source to substrate voltage V_{SB} increases. With reference to the proposed squaring circuit shown in Figure (3.11), we can see that the bulk of all transistors except M2 and M4 are connected to the source, hence the source-bulk voltage (V_{SB}) will be zero. Thus, these transistors will have $V_{TH}=V_{THO}$. To avoid the body effect, the PMOS transistors M2 and M4 are placed in separated wells to make $V_{SB}=0$ and hence $V_{TH}=V_{THO}$. In the proposed circuit if we consider that a worst case in which transistors M1 and M4 in the MTL have threshold voltage mismatch such that:

$$V_{GS1} \approx \frac{I_{D1}\theta}{\beta} + \sqrt{\frac{2I_{D1}}{\beta}} + \left(V_{TH} + \Delta V_{TH}\right) \tag{3.114}$$

$$V_{GS4} \approx \frac{I_{D4}\theta}{\beta} + \sqrt{\frac{2I_{D4}}{\beta}} + \left(V_{TH} - \Delta V_{TH}\right) \tag{3.115}$$

where ΔV_{TH} is mismatch term between V_{TH1}, V_{TH4}

Combining equations (3.86), (3.114) and (3.115) yield:

$$\Delta V_{TH} + \frac{I_{D1}\theta}{2\beta} + \sqrt{\frac{I_{D1}}{\beta}} + \frac{I_{D2}\theta}{2\beta} + \sqrt{\frac{I_{D2}}{\beta}} = \frac{I_{D3}\theta}{\beta} + \sqrt{\frac{2I_{D3}}{\beta}} + \frac{I_{D4}\theta}{\beta} + \sqrt{\frac{2I_{D4}}{\beta}} - \Delta V_{TH} \tag{3.116}$$

Following the same analysis as before, it is easy to show that:

$$\Delta V_{TH} + 2\sqrt{\frac{I_B}{\beta}} = \sqrt{\frac{I_{D3}}{\beta}} + \sqrt{\frac{I_{D4}}{\beta}} - \Delta V_{TH} \tag{3.117}$$

With reference to Figure (3.10), the drain current of M3 is given by:

$$I_{D3} = I_{D4} + I_X \tag{3.118}$$

Substituting equation (3.118) into equation (3.117), squaring both sides twice and ignoring higher orders, the current I_{D3} can be expressed as:

$$I_{D3} = \frac{I_X^2}{8I_B\left(1+2\Delta V_{TH}\sqrt{\beta I_B}\right)} + \frac{I_X + I_B}{2\left(1+2\Delta V_{TH}\sqrt{\beta I_B}\right)} + \frac{\Delta V_{TH}\sqrt{\beta I_B}\left(I_X + 2I_B\right)}{I_B\left(1+2\Delta V_{TH}\sqrt{\beta I_B}\right)} \tag{3.119}$$

But $\left(2\Delta V_{TH}\sqrt{\beta I_B} << 1\right)$, equation (3.119) can be rewritten as:

$$I_{D3} = \frac{I_X^2}{8I_B} + \frac{I_X + I_B}{2} + \Delta V_{TH}\sqrt{\frac{\beta}{I_B}} \times \left(I_X + 2I_B\right) \tag{3.120}$$

The second term to the right of equation (3.120) is subtracted using transistors M10 and M11 and the output current is given by:

$$I'_{out} = \frac{I_X^2}{8I_B} + \Delta V_{TH}\sqrt{\frac{\beta}{I_B}} \times \left(I_X + 2I_B\right) \tag{3.121}$$

The absolute error can be written as:

$$I_{error} = \left|I_{out} - I'_{out}\right| = \left|\Delta V_{TH}\sqrt{\frac{\beta}{I_B}} \times \left(I_X + 2I_B\right)\right| \tag{3.122}$$

To evaluate the error due to threshold mismatch in equation (3.122), we consider I_x=40μA, I_B=60μA, β=86μA/V^2, L=0.2μm, and $\Delta V_{TH} = \frac{0.1\times 4.1\times 10^{-9}}{\sqrt{5\times 10^{-6}\times 0.2\times 10^{-6}}} = 0.41mV$, then the maximum error is 78.5nA which corresponds to 2.3%.

Again, with reference to Figure (3.11), the drain currents of M9 is forced to be equal the summation of drain currents of M3 and M4 and hence the effect of carrier mobility reduction in MTL loop can be canceled, so study of threshold mismatch for transistor M9 is critical in determining the accuracy of the proposed circuit. The gate-source potential for M7 and M 9 is given by:

$$V_{GS7} = \sqrt{\frac{2I_B}{2\beta}} + V_{TH} \tag{3.123}$$

$$V_{GS9} = \sqrt{\frac{2I_{D9}}{2\beta}} + V_{TH} + \Delta V_{TH} \tag{3.124}$$

With reference to Figure (3.11), V_{GS7}= V_{GS9}, then:

$$\sqrt{\frac{I_B}{\beta}} + V_{TH} = \sqrt{\frac{I_{D9}}{\beta}} + V_{TH} + \Delta V_{TH} \tag{3.125}$$

Equation (3.125) can be rewritten as:

$$\sqrt{\frac{I_B}{\beta}} = \sqrt{\frac{I_{D9}}{\beta}} + \Delta V_{TH} \tag{3.126}$$

Squaring both sides and ignoring higher order terms of ΔV_{TH}, the current of I_{D9} can be expressed as:

$$I_{D9} = I_B - 2\Delta V_{TH}\sqrt{\beta \times I_B} \tag{3.127}$$

With reference to Figure (3.11), the current I_{D9} can be written as:

$$I_{D9} = I_{D3} + I_{D4} = I_B - 2\Delta V_{TH}\sqrt{\beta \times I_B} \tag{3.128}$$

Combining equations (3.91) and (3.128) to get:

$$2\sqrt{I_B} + 2\theta\Delta V_{TH}\sqrt{I_B} = \sqrt{2I_{D3}} + \sqrt{2I_{D4}} \tag{3.129}$$

Substituting equation (3.92) into equation (3.129) and squaring both side twice and ignoring higher order terms, the current I_{D3} can be expressed as:

$$I_{D3} = \frac{I_X^2}{8I_B(1+2\theta\Delta V_{TH})} + \frac{I_X + I_B}{2(1+2\theta\Delta V_{TH})} + \frac{\theta\Delta V_{TH}(2I_B + I_X)}{(1+2\theta\Delta V_{TH})} \tag{3.130}$$

But $(2\theta\Delta V_{TH} << 1)$, equation (3.130) can be written as:

$$I_{D3} = \frac{I_X^2}{8I_B} + \frac{I_X + I_B}{2} + \theta\Delta V_{TH}(2I_B + I_X) \tag{3.131}$$

The second term to the right of equation (3.131) is subtracted using transistors M10 and M11 and the output current is given by:

$$I'_{out} = \frac{I_X^2}{8I_B} + \theta\Delta V_{TH}(2I_B + I_X) \tag{3.132}$$

The absolute error can be written as:

$$I_{error} = |I_{out} - I'_{out}| = |\theta\Delta V_{TH}(I_X + 2I_B)| \tag{3.133}$$

As an example, if I_x=40μA, I_B=60μA, θ=0.25V^{-1}, L=0.2μm, and $\Delta V_{TH} = 0.41mV$, the maximum current error can be written as: $I_{error} = 16.4nA$ which is equivalent to 0.5%.

This means the proposed circuit is a little sensitive to mismatch in the threshold voltage. To conclude, this mismatch in parameters will degrade the accuracy of the design and some layout techniques used to minimize such mismatch.

Simulation Result of the Threshold Voltage Mismatch

It is well know that mismatch will degrade the accuracy of the design. In the proposed circuit, study of threshold mismatch for MTL was carried out for M1 and M4 as it is the most important block. Mont Carlo analysis was carried out for 100 times (Monte=100). The simulation result shown in Figure (3.16) indicates that the corresponding maximum deviation of the output current is about 1.3%. It is clear that the circuit is almost insensitive to threshold voltage mismatch.

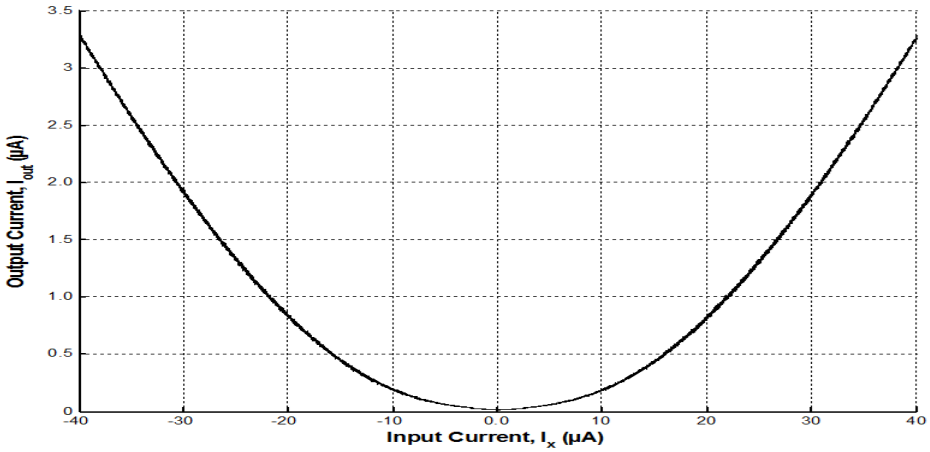

Figure 3.16 Monte Carlo analysis with Gaussian distribution for threshold variation for the squaring circuit

3.3.3.4 Channel Length Mismatch

The same analysis can be performed on mismatch in channel length parameter *L*. if we consider transistors M1 and M4 have channel length mismatch and assuming perfect match for all other parameters, the gate-source potential of M1 and M4 can be written as:

$$V_{GS1} \approx \frac{I_{D1}\theta_1\left(\frac{L+\Delta L}{L}\right)}{\beta_1} + \sqrt{\frac{2I_{D1}\left(\frac{L+\Delta L}{L}\right)}{\beta_1}} + V_{TH} \tag{3.134}$$

$$V_{GS4} \approx \frac{I_{D4}\theta_4\left(\frac{L-\Delta L}{L}\right)}{\beta_4} + \sqrt{\frac{2I_{D4}\left(\frac{L-\Delta L}{L}\right)}{\beta_4}} + V_{TH} \tag{3.135}$$

where, $\beta_i = k'_{pi}\frac{W}{L}$ is transconductance parameter for transistor M_i;

Combining equations (3.86), (3.134) and (3.135) yield:

$$\frac{I_{D1}\theta_1\left(\frac{L+\Delta L}{L}\right)}{\beta_1} + \sqrt{\frac{2I_{D4}\left(\frac{L+\Delta L}{L}\right)}{\beta_1}} + \frac{I_{D2}\theta_2}{\beta_2} + \sqrt{\frac{2I_{D2}}{\beta_2}} = \frac{I_{D3}\theta_3}{\beta_3} + \sqrt{\frac{2I_{D3}}{\beta_3}} + \frac{I_{D1}\theta_4\left(\frac{L-\Delta L}{L}\right)}{\beta_4} + \sqrt{\frac{2I_{D4}\left(\frac{L-\Delta L}{L}\right)}{\beta_4}} \tag{3.136}$$

Following the same analysis as before, it is easy to show that;

$$\left(\frac{\theta\Delta L}{2L\sqrt{\beta}}I_B + \frac{\theta\Delta L}{L\sqrt{\beta}}I_{D3} + \frac{\theta\Delta L}{L\sqrt{\beta}}I_x\right) + \left(\sqrt{I_B\left(\frac{L+\Delta L}{L}\right)} + \sqrt{I_B}\right) = \left(\sqrt{2I_{D3}} + \sqrt{2I_{D4}\left(\frac{L-\Delta L}{L}\right)}\right) \tag{3.137}$$

Squaring both sides and ignoring higher order terms, equation (3.137) can be rewritten as:

$$I_B + I_B\left(1+\frac{\Delta L}{L}\right) + 2I_B\sqrt{1+\frac{\Delta L}{L}} + \left\{\begin{array}{l}\frac{\theta\Delta L}{L\sqrt{\beta}}\sqrt{I_B\left(1+\frac{\Delta L}{L}\right)}\left(I_B+2I_{D3}-2I_x\right) \\ +\frac{\theta\Delta L}{L\sqrt{\beta}}\sqrt{I_B}\left(I_B+2I_{D3}-2I_x\right)\end{array}\right\} = \left\{\begin{array}{l}2I_{D3}+4\sqrt{I_{D3}I_{D4}\left(1-\frac{\Delta L}{L}\right)} \\ +2I_{D4}\left(1-\frac{\Delta L}{L}\right)\end{array}\right\} \tag{3.138}$$

But$\left(\frac{\Delta L}{L} << 1\right)$, then equation (3.138) can be written as:

$$\left(4I_B - 4I_{D3} + 2I_x\right) + \left(\frac{2\theta\Delta L}{L\sqrt{\beta}}\sqrt{I_B}\left[I_B + 2I_{D3} - 2I_x\right]\right) = 4\sqrt{I_{D3}I_{D4}} \tag{3.139}$$

If both sides are squared again and the higher order terms are ignored, then equation (3.139) can be rewritten as:

$$4I_x^2+16I_xI_B\left(1-\frac{3\theta\Delta L}{2L\sqrt{\beta}}\sqrt{I_B}\right)+16I_B^2\left(1+\frac{\theta\Delta L}{L\sqrt{\beta}}\sqrt{I_B}\right)-\frac{16\theta\Delta L}{L\sqrt{\beta}}I_x^2\sqrt{I_B}+\left\{\begin{matrix}16I_{D3}^2\left(1-\frac{2\theta\Delta L}{L\sqrt{\beta}}\sqrt{I_B}\right)\\-32I_{D3}I_B\left(1-\frac{\theta\Delta L}{2L\sqrt{\beta}}\sqrt{I_B}\right)\\-16I_{D3}I_x\left(1-\frac{3\theta\Delta L}{L\sqrt{\beta}}\sqrt{I_B}\right)\end{matrix}\right\}=16I_{D3}I_{D4} \quad (3.140)$$

Assuming $\left(\frac{3\theta\Delta L}{L\sqrt{\beta}}\sqrt{I_B}<<1\right)$ and substituting $\left(I_{D4}=I_{D3}-I_x\right)$ the current I_{D3} can be expressed as:

$$I_{D3}=\frac{I_x^2}{8I_B}+\frac{I_x+I_B}{2}-\frac{\theta\Delta L}{2L\sqrt{\beta\times I_B}}I_x^2 \quad (3.141)$$

The second term to the right of equation (3.141) is subtracted using transistors M10 and M11and then the output current is given as:

$$I'_{out}=\frac{I_x^2}{8I_B}-\frac{\theta\Delta L}{2L\sqrt{\beta\times I_B}}I_x^2 \quad (3.142)$$

The absolute error can be written as:

$$I_{error}=\left|I_{out}-I'_{out}\right|=\left|\frac{\theta\Delta L}{2L\sqrt{\beta\times I_B}}I_x^2\right| \quad (3.143)$$

To evaluate the error due to channel length mismatch in equation (3.143), we consider I_x=40μA, I_B=60μA, θ=0.25V^{-1}, β=86μA/V^2, L=0.2μm and $\Delta L=0.004\mu m$, then the maximum current error is 55.6nA which corresponds to a relative error of 1.7%.

However, study of channel length mismatch for transistors M7 and M9 is also critical in determining the accuracy of the proposed circuit. Assuming this mismatch, the gate-source potential for M7 and M 9 is given by:

$$V_{GS7} = \sqrt{\frac{2I_B}{2\beta}} + V_{TH} \tag{3.144}$$

$$V_{GS9} = \sqrt{\frac{2I_{D9}\left(\frac{L+\Delta L}{L}\right)}{2\beta}} + V_{TH} \tag{3.145}$$

With reference to Figure (3.11), $V_{GS7} = V_{GS9}$, then:

$$\sqrt{\frac{I_B}{\beta}} + V_{TH} = \sqrt{\frac{I_{D9}\left(\frac{L+\Delta L}{L}\right)}{\beta}} + V_{TH} \tag{3.146}$$

Equation (3.146) can be rewritten as:

$$\sqrt{\frac{I_B}{\beta}} = \sqrt{\frac{I_{D9}\left(\frac{L+\Delta L}{L}\right)}{\beta}} \tag{3.147}$$

Then, the current of transistor M9 expressed as:

$$I_{D9} = I_{D3} + I_{D4} = I_B\left(\frac{L}{L+\Delta L}\right) = I_B\left(\frac{1}{1+\frac{\Delta L}{L}}\right) \tag{3.148}$$

But $\left(\frac{\Delta L}{L} << 1\right)$, then equation (3.148) can be rewritten as:

$$I_{D9} \approx I_B\left(1-\frac{\Delta L}{L}\right) \approx I_B - \frac{\Delta L}{L} I_B \tag{3.149}$$

Combining equations (3.91) and (3.149) to get:

$$\frac{\theta \Delta L}{L\sqrt{\beta}} I_B + 2\sqrt{I_B} = \sqrt{2I_{D3}} + \sqrt{2I_{D4}} \tag{3.150}$$

Substituting equation (3.92) into equation (3.150) and squaring both side twice and ignoring higher order terms, then equation (3.150) can be rewritten:

$$4I_x^2+16I_xI_B\left(1+\frac{\theta\Delta L}{L\sqrt{\beta}}\sqrt{I_B}\right)+16I_B^2+\frac{32\theta\Delta L}{L\sqrt{\beta}}I_B^2\sqrt{I_B}=32I_BI_{D3}\left(1+\frac{\theta\Delta L}{L\sqrt{\beta}}\sqrt{I_B}\right) \tag{3.151}$$

But$\left(\frac{\theta\Delta L}{L\sqrt{\beta}}\sqrt{I_B}<<1\right)$, equation (3.151) can be rewritten as:

$$I_{D3}=\frac{I_x^2}{8I_B}+\frac{I_x+I_B}{2}+\frac{\theta\Delta L}{L\sqrt{\beta}}I_B\sqrt{I_B} \tag{3.152}$$

The second term to the right of equation (3.152) is subtracted using transistors M10 and M11 and then the output current is given as:

$$I'_{out}=\frac{I_x^2}{8I_B}+\frac{\theta\Delta L}{L\sqrt{\beta}}I_B\sqrt{I_B} \tag{3.153}$$

which results in an absolute error given by:

$$I_{error}=\left|I_{out}-I'_{out}\right|=\left|\frac{\theta\Delta L}{L\sqrt{\beta}}I_B\sqrt{I_B}\right| \tag{3.154}$$

To evaluate the error due to channel length mismatch considering the worst case of all parameters in equation (3.154) is, for example, $I_B=60\mu A$, $\theta=0.25V^{-1}$, $\beta=86\mu A/V^2$, $L=0.2\mu m$ and $\Delta L=0.004\mu m$, The maximum error is 0.25µA which is equivalent to 7.5%.

It is clear that the output current of the proposed squaring circuit is very bad performance with channel length mismatch. To avoid this deviation, an accurate fabrication process is highly necessary.

Simulation Result of the Channel Length Mismatch

Also the channel length mismatch for MTL was carried out for transistors M1 and M4. Mont Carlo analysis was carried out for 100 times (Monte=100) with mean value of 0.2µm and three sigma variation of 0.012µm (0.02 channel length variation). The simulation result shown in Figure (3.17) indicates that the corresponding maximum deviation of the output current is about 2%. It is clear that the maximum error results due to the channel length mismatch is within the acceptable range.

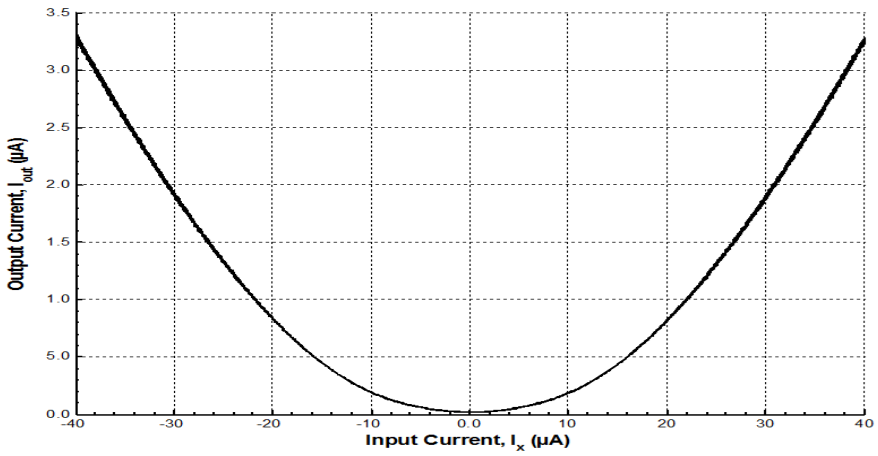

Figure 3.17 Monte Carlo analysis with Gaussian distribution for the squaring circuit

Summary of the comparison is shown in table (3.5). The performance of the proposed squaring circuit compared with recently published works. It is clear that the proposed circuit has a better performance in terms of relative error, bandwidth and silicon area. However, the proposed circuit is simulated using 0.18µm CMOS technology and it is used transistors with shorter channel-length (L=0.2µm) in comparison with previously published works shown in table (3.5) which used long channel-length transistors to

reduce/cancel the error caused by carrier mobility reduction and channel length modulation, and hence improve the accuracy of the designed circuits.

Table 3.5 Comparison between the proposed squaring and previously reported works

Ref.	Public Year	Type (In/Out)	Tech. (µm)	Minim. L (µm)	Supply Voltage (V)	Input Range (µA)	Power Cons. (µW)	Relative Error (%)	-3 dB Frequency (MHz)	Area (μm^2)
[51]	2008	VI/CO	0.25	1.2	3.3	±1.0V	90	3.0	200	340
[61]	2011	CI/CO	0.25	0.5	1.4	±40	72.6	1.9	0.03	
[62]	2007	CI/CO	0.35	0.7	3.0	7.0	-	-	50	1500
[63]	2011	CI/CO	0.35	2.0	-	40	-	-	-	-
This Work	**2013**	**CI/CO**	**0.18**	**0.2**	**1.5**	**±40**	**326**	**1.2**	**340**	**76.5**

3.4 Current-mode Multiplying Circuit

In this section, the proposed current-mode multiplying circuit will be discussed. Simulation results and mismatch analysis will be presented. Finally, summary of performance comparison between the propose circuit and previously published work will be given.

3.4.1 Proposed Current-mode Multiplying Circuit

The proposed current-mode multiplying circuit is shows Figure (3.21). The principle of operation of the multiplier is based on the square-difference which is defined by the following formula:

$$(X+Y)^2-(X-Y)^2=4XY \tag{3.155}$$

The proposed squaring circuit shown in Figure (3.10) is used to realize the proposed multiplying circuit. With reference to Figure (3.81), the circuit consists of two squaring circuits and one subtracting circuit. The two squaring circuits with input functions *(X+Y)* and *(X-Y)* can provide the squaring function $(X+Y)^2$ and $(X-Y)^2$ respectively. The subtracting circuit will produce the difference of the two squared signals to get at the end the multiplying function. To reduce the number of transistors of the circuit designed, transistors M1 and M2 are used as common transistors between tow squaring circuits.

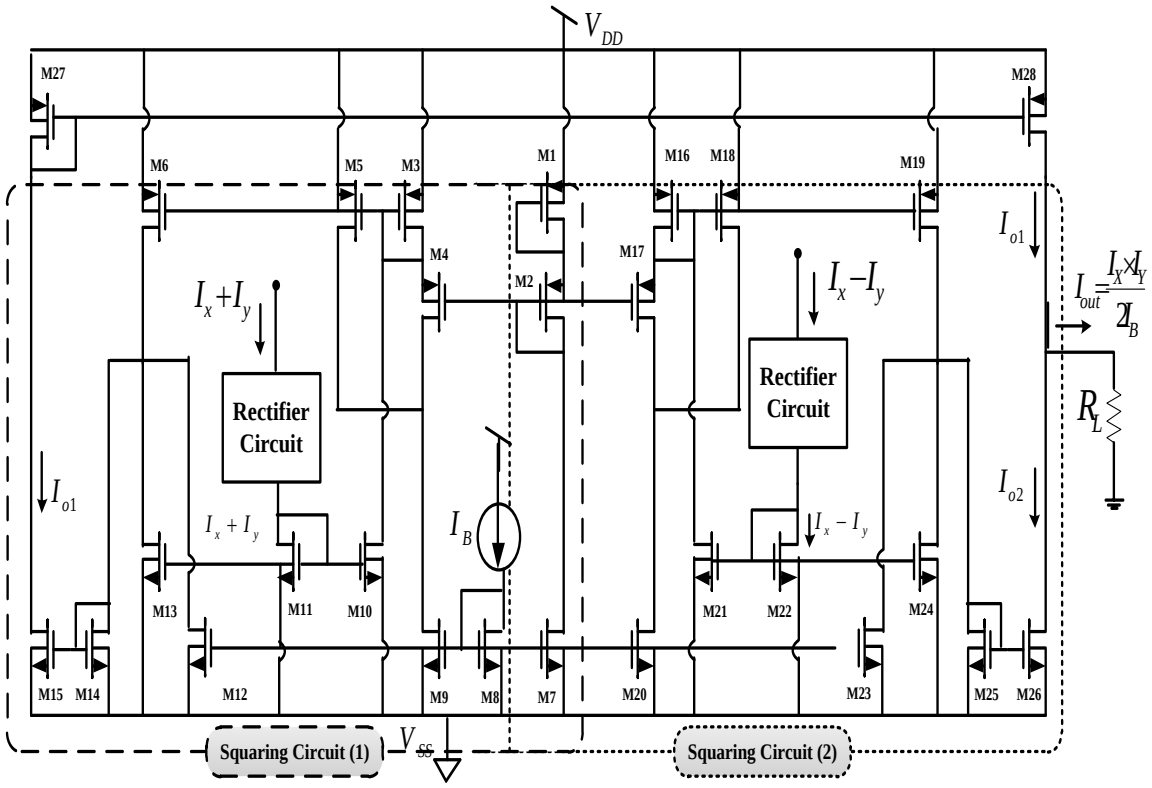

Figure 3.18 Proposed current-mode multiplied circuit

According to the circuit schematic in Figure (3.81), the output current of the first squaring circuit is given by:

$$I_{o1} = \frac{(I_x + I_y)^2}{8I_B} \tag{3.156}$$

And the output current of the second squaring circuit is given by:

$$I_{o2} = \frac{(I_x - I_y)^2}{8I_B} \tag{3.157}$$

The output currents of the multiplier circuit can be written as:

$$I_{out} = I_{O1} - I_{O2} = \frac{(I_x + I_y)^2}{8I_B} - \frac{(I_x - I_y)^2}{8I_B} = \frac{I_x I_y}{2I_B} \tag{3.158}$$

Equation (3.158) can be rewritten as:

$$I_{out} = k(I_x \times I_y) \tag{3.159}$$

where, $k = \frac{1}{2I_B}$

It is clear that equation (3.159) implements a four quadrant current-mode multiplying circuit with compensation for error due to carrier mobility reduction.

3.4.2 Simulation Results

The proposed multiplying circuit was simulated using Tanner T-spice in 0.18µm CMOS process technology. The bias current is *60µA* and the input currents *(I_x, I_y)* are swept from *-20* to *20µA*. The circuit is operated from *1.5V* DC supply voltage and the aspect ratios of all transistors used are listed in table (3.6). The output current was measured by forcing it through a load resistor R_L*=10kΩ*.

Table 3.6 Transistor aspect ratios of the multiplying circuit

W/L (µm)		W/L (µm)		W/L (µm)		W/L (µm)		W/L (µm)	
M1	5.0/0.2	M7	5.0/0.2	M13	2.5/0.2	M19	2.5/0.2	M25	0.75/0.75
M2	5.0/0.2	M8	5.0/0.2	M14	0.75/0.75	M20	5.0/0.2	M26	0.75/0.75
M3	2.5/0.2	M9	5.0/0.2	M15	0.75/0.75	M21	5.0/0.2	M27	0.75/07.5
M4	2.5/0.2	M10	5.0/0.2	M16	2.5/0.2	M22	5.0/0.2	M28	0.75/0.75
M5	2.5/0.2	M11	5.0/0.2	M17	2.5/0.2	M23	2.5/0.2		
M6	2.5/0.2	M12	2.5/0.2	M18	2.5/0.2	M24	2.5/0.2		

The DC transfer characteristic of the multiplying circuit is shown in Figure (3.19). It is clear from the plot that the simulated result confirms the functionality of the developed design. Plot of the error between calculated and simulated results is shown in Figure (3.20). The maximum relative error is 1.8% and the maximum power consumption is 700µW.

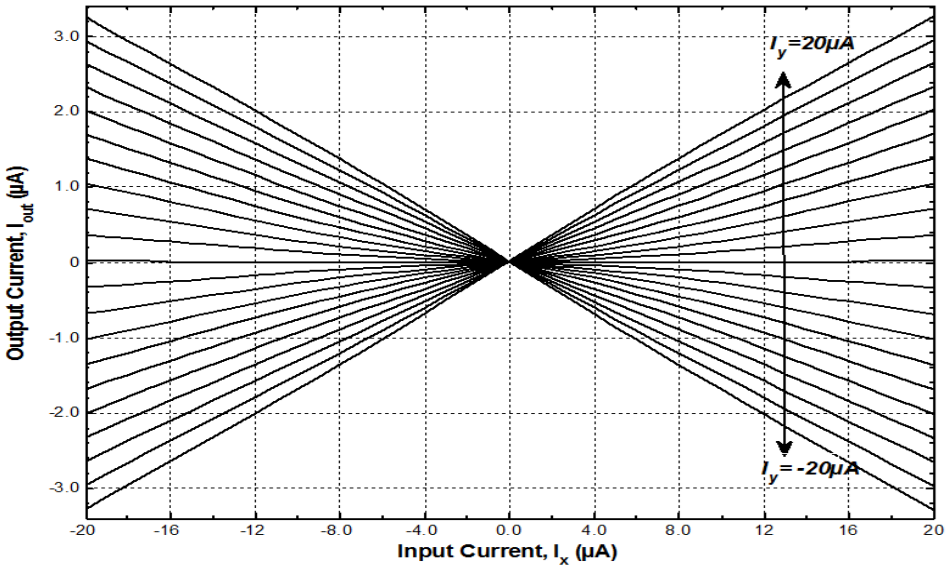

Figure 3.19 Simulation result for DC transfer characteristics of the multiplying Circuit

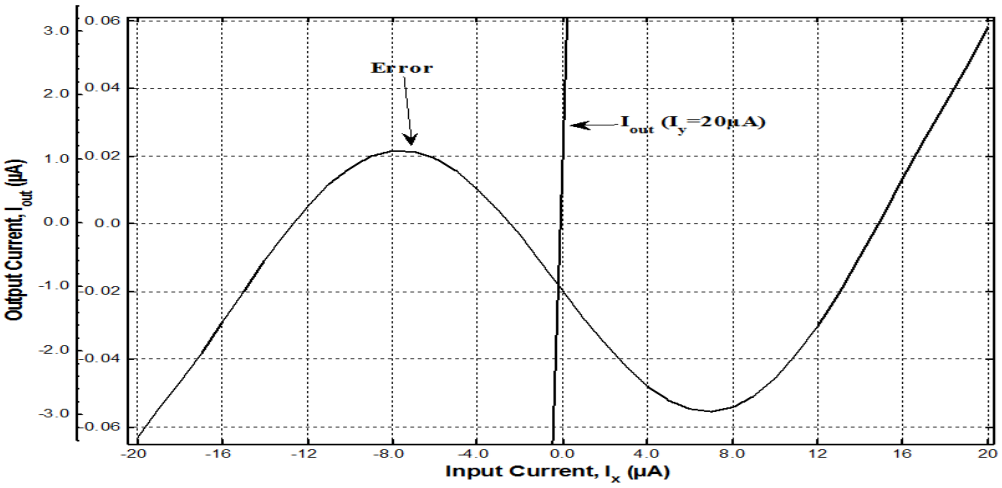

Figure 3.20 The error of the proposed multiplying circuit

The transient analysis was carried out when in the inputs *Ix* and *Iy* are sinusoidal signal with *1MHz* frequency and different amplitude. Simulation result shown in Figure (3.21) confirms the functionality of the design.

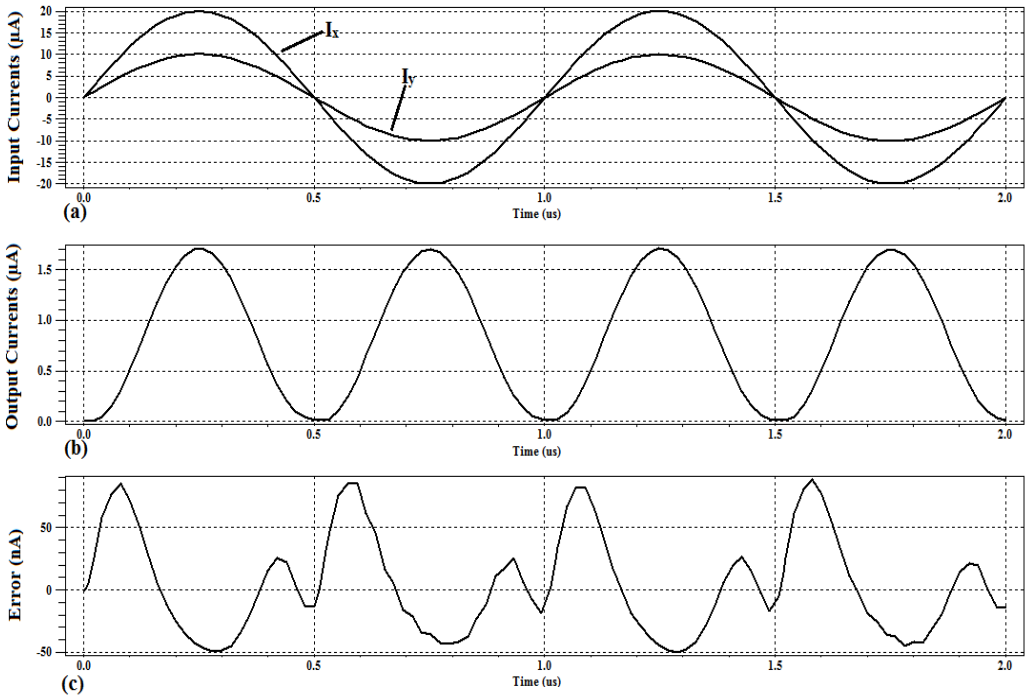

Figure 3.21 Simulation for transient analysis (a) Input signal (b) Output signal (c) Error

Simulation for temperature analysis was carried out. The temperature was swept from -25°C to 75° C in steps of 50°C. The simulation result shown in Figure (3.22) confirms that the proposed circuit is sensitive to temperature variation.

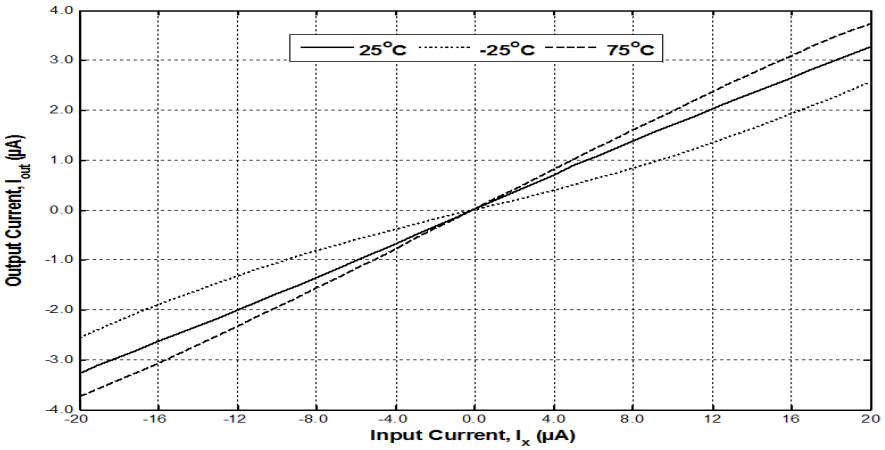

Figure 3.22 Simulation result for temperature variation of the multiplying Circuit

The circuit was simulated for the frequency response. An AC input signal is applied to I_x and I_y=*40µA* DC and the frequency is swept from *10Hz* to *10GHz*. Simulation result shown in Figure (3.23) indicates the upper -3dB frequency is *230MHz*.

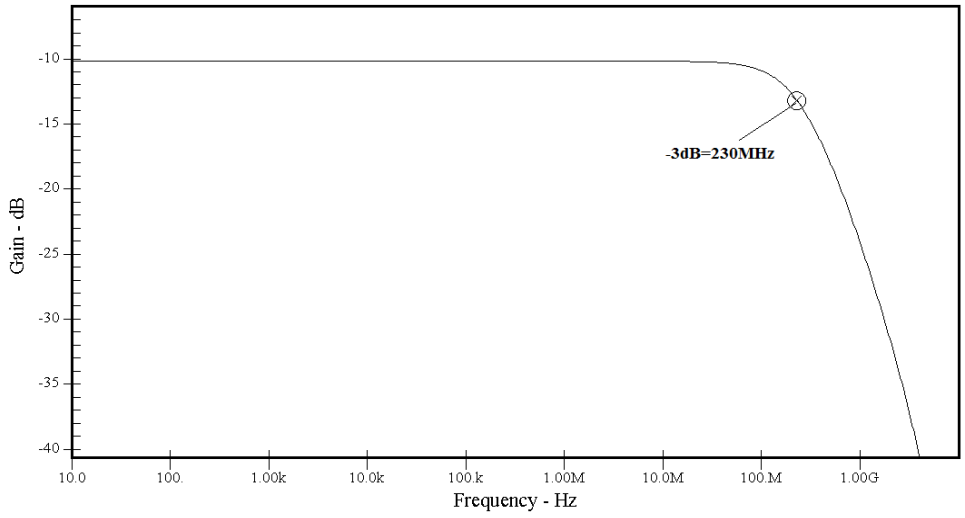

Figure 3.23 Frequency response of the proposed multiplying circuit

The proposed multiplying circuit can be used as Amplitude Modulation (AM). To simulate this application, two signal are used, one as carrier with 10MHz frequency and the other as signal with 500 kHz. The amplitude of both inputs is $40\mu A_{p-p}$. Simulation results for the input signal and amplitude modulator (AM) are shown in Figure (3.24).

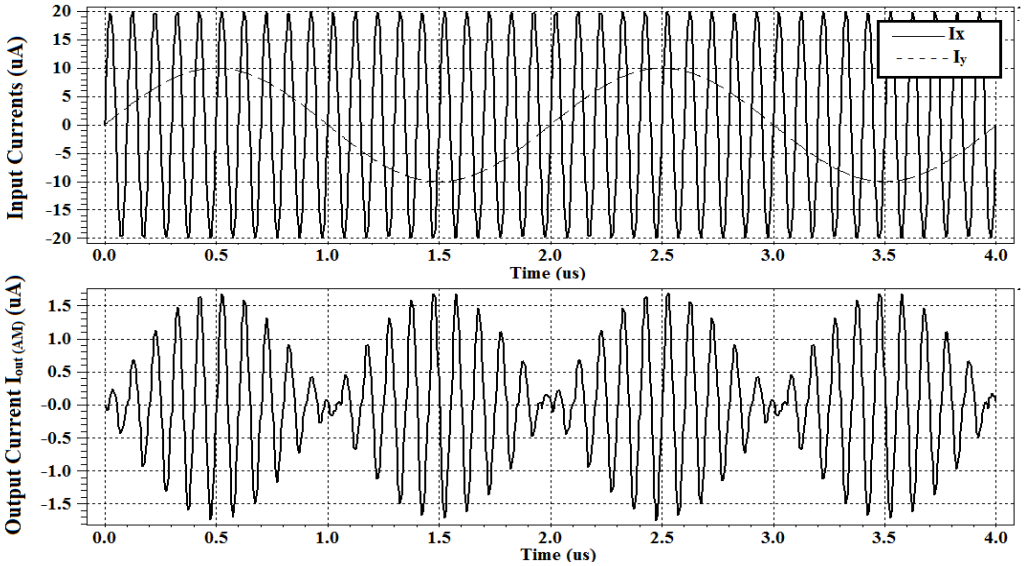

Figure 3.24 Modulated ac output current of the multiplying as amplitude modulation

3.4.3 Mismatch Analysis

In this section, the mismatch analysis of the proposed multiplying circuit will include the mobility parameter, transconductance parameter, threshold voltage and channel length of transistors in MTL will be carried out.

3.4.3.1 Mobility Parameter Mismatch

If it is assumed that the mobility parameter of transistors M1-M4, M16 and M17 of the proposed multiplying circuit is not perfectly matched, the output currents of the squaring can be written as:

$$I'_{o1} = \frac{(I_x + I_y)^2}{8I_B} + \frac{2\Delta\theta}{\sqrt{\beta}} I_B \sqrt{I_B} \tag{3.160}$$

$$I'_{o2} = \frac{(I_x - I_y)^2}{8I_B} + \frac{2\Delta\theta}{\sqrt{\beta}} I_B \sqrt{I_B} \tag{3.161}$$

The output current of the proposed multiplying circuit can be written as:

$$I'_{out} = I'_{o1} - I'_{o2} \tag{3.162}$$

Combining equations (3.160), (3.161) and (3.162) to get:

$$I'_{out} = \frac{(I_x + I_y)^2 - (I_x - I_y)^2}{8I_B} + \left(\frac{2\Delta\theta}{\sqrt{\beta}} I_B \sqrt{I_B}\right) - \left(\frac{2\Delta\theta}{\sqrt{\beta}} I_B \sqrt{I_B}\right) \tag{3.163}$$

Equation (3.163) can be rewritten as:

$$I'_{out} = \frac{I_x I_y}{2I_B} \tag{3.164}$$

The absolute error can be written as:

$$I_{error} = |I_{out} - I'_{out}| = \left|\left(\frac{I_x I_y}{2I_B}\right) - \left(\frac{I_x I_y}{2I_B}\right)\right| = 0 \tag{3.165}$$

The advantage of using the function $(X+Y)^2 - (X-Y)^2$ in the multiplier circuit is to cancel the offset error by eliminating the second term in equations (3.160) and (3.161). Consequently the proposed design is insensitive to the carrier mobility parameter mismatch.

3.4.3.2 Transconductance Parameter Mismatch

The same analysis can be performed on the transconductance parameter, the output currents of the squaring can be written as:

$$I'_{o1} = \frac{(I_x + I_y)^2}{8I_B} + \frac{2\theta\Delta\beta}{\beta\sqrt{\beta}} I_B \sqrt{I_B} \tag{3.166}$$

$$I'_{o2} = \frac{(I_x - I_y)^2}{8I_B} + \frac{2\theta\Delta\beta}{\beta\sqrt{\beta}} I_B \sqrt{I_B} \tag{3.167}$$

Combining equations (3.162), (3.166) and (3.167) to get:

$$I'_{out} = \frac{(I_x + I_y)^2 - (I_x - I_y)^2}{8I_B} + \left(\frac{2\theta\Delta\beta}{\beta\sqrt{\beta}} I_B \sqrt{I_B}\right) - \left(\frac{2\theta\Delta\beta}{\beta\sqrt{\beta}} I_B \sqrt{I_B}\right) \tag{3.168}$$

Equation (3.168) can be rewritten as:

$$I'_{out} = \frac{I_x I_y}{2I_B} \tag{3.169}$$

The absolute error can be written as:

$$I_{error} = \left|I_{out} - I'_{out}\right| = 0 \tag{3.170}$$

This means that the mismatch in transconductance parameter will not degrade the accuracy of the proposed design.

3.4.3.3 Threshold Voltage Mismatch

In the proposed multiplying circuit shown in Figure (3.21), if we consider that a worst case in which transistors M1and M4 in the MTL have threshold voltage mismatch. The output currents of the squarer can be written as:

$$I'_{o1} = \frac{(I_x + I_y)^2}{8I_B} + \Delta V_{TH}\sqrt{\frac{\beta}{I_B}} \times (I_x + I_y + 2I_B) \tag{3.171}$$

$$I'_{o2} = \frac{(I_x - I_y)^2}{8I_B} + \Delta V_{TH}\sqrt{\frac{\beta}{I_B}} \times (I_x - I_y + 2I_B) \tag{3.172}$$

Combining equations (3.162), (3.171) and (3.172) to get:

$$I'_{out} = \frac{(I_x + I_y)^2 - (I_x - I_y)^2}{8I_B} + \Delta V_{TH}\sqrt{\frac{\beta}{I_B}}\left[(I_x + I_y + 2I_B) - (I_x - I_y + 2I_B)\right] \tag{3.173}$$

Equation (3.173) can be rewritten as:

$$I'_{out} = \frac{I_x I_y}{2I_B} + 2\Delta V_{TH}\sqrt{\frac{\beta}{I_B}} \times I_y \tag{3.174}$$

which results in an absolute error given by:

$$I_{error} = \left|I_{out} - I'_{out}\right| = \left|2\Delta V_{TH}\sqrt{\frac{\beta}{I_B}} \times I_y\right| \tag{3.175}$$

The current error quantity in equation (2.175) can be calculated such as: I_y=*20μA*, I_B=*60μA*, β=*86μA/V*^{2} and $\Delta V_{TH} = 0.41mV$, then the maximum error is *19.6nA* which is corresponds to 0.6%.

However, in the proposed circuit, study of threshold mismatch for transistors M9 and M20 are critical in determining the accuracy of the proposed circuit because cancelation of the effect of the carrier mobility reduction is based on the assumption transistors are matched. If there is a mismatch, the output currents of the squaring circuit can be written as:

$$I'_{out1} = \frac{(I_x + I_y)^2}{8I_B} + \theta \Delta V_{TH}(2I_B + I_X + I_y) \tag{3.176}$$

$$I'_{out2} = \frac{(I_x - I_y)^2}{8I_B} + \theta \Delta V_{TH}(2I_B + I_x - I_y) \tag{3.177}$$

Combining equations (3.162), (3.176) and (3.177) to get:

$$I'_{out} = \frac{(I_x + I_y)^2 - (I_x - I_y)^2}{8I_B} + \theta \Delta V_{TH}\left[(2I_B + I_x + I_y) - (2I_B + I_x - I_y)\right] \tag{3.178}$$

Equation (3.178) can be rewritten as:

$$I'_{out} = \frac{I_x I_y}{2I_B} + 2\theta \Delta V_{TH} I_y \tag{3.179}$$

which results in an absolute error given by:

$$I_{error} = \left|I_{out} - I'_{out}\right| = \left|2\theta \Delta V_{TH} I_y\right| \tag{3.180}$$

As an example, if I_y=*20μA*, θ=*0.25V*$^{-1}$ *and* $\Delta V_{TH} = 0.41mV$, the maximum error is *4.1nA* which is equivalent to *0.12%*. It is clear that the proposed design has very good performance with threshold voltage mismatch.

3.4.3.4 Channel Length Mismatch

With reference to Figure (3.24), if we consider the mismatch in transistors M1and M4, the output currents of the squaring circuit can be written as:

$$I'_{out1} = \frac{\left(I_x + I_y\right)^2}{8I_B} - \frac{\theta\Delta L}{2L\sqrt{\beta \times I_B}}\left(I_x + I_y\right)^2 \tag{3.181}$$

$$I'_{out2} = \frac{\left(I_x - I_y\right)^2}{8I_B} - \frac{\theta\Delta L}{2L\sqrt{\beta \times I_B}}\left(I_x - I_y\right)^2 \tag{3.182}$$

Combining equations (3.160), (3.181) and (3.182), the output current of the proposed multiplying circuit can be written as:

$$I'_{out} = \frac{\left(I_x + I_y\right)^2 - \left(I_x - I_y\right)^2}{8I_B} - \frac{\theta\Delta L}{2L\sqrt{\beta \times I_B}}\left(\left(I_x + I_y\right)^2 - \left(I_x - I_y\right)^2\right) \tag{3.183}$$

Equation (3.183) can be rewritten as:

$$I'_{out} = \frac{I_x I_y}{2I_B} - \frac{2\theta\Delta L}{L\sqrt{\beta \times I_B}} I_x I_y \tag{3.184}$$

The absolute error is given as:

$$I_{error} = \left|I_{out} - I'_{out}\right| = \left|\frac{2\theta\Delta L}{L\sqrt{\beta \times I_B}} I_x I_y\right| \tag{3.185}$$

To evaluate the error due to channel length mismatch in equation (3.185), we consider I_x=20μA, I_y=20μA, β=86μA/V^2, I_B=60μA, θ =0.25V^{-1}, L=0.2μm and $\Delta L = 0.004\mu m$, then the maximum error is 55.6nA which corresponds to maximum error of 1.7%.

Also, if there is mismatch between M9 and M20, the output currents of the squaring circuit can be written as:

$$I'_{out1} = \frac{(I_x + I_y)^2}{8I_B} + \frac{\theta \Delta L}{L\sqrt{\beta}} I_B \sqrt{I_B} \tag{3.186}$$

$$I'_{out2} = \frac{(I_x - I_y)^2}{8I_B} + \frac{\theta \Delta L}{L\sqrt{\beta}} I_B \sqrt{I_B} \tag{3.187}$$

Combining equations (3.160), (3.186) and (3.187), the output current of the proposed multiplying circuit can be written as:

$$I'_{out} = \frac{(I_x + I_y)^2 - (I_x - I_y)^2}{8I_B} + \left(\frac{\theta \Delta L}{L\sqrt{\beta}} \sqrt{I_B} \right) - \left(\frac{\theta \Delta L}{L\sqrt{\beta}} \sqrt{I_B} \right) \tag{3.188}$$

Equation (3.188) can be rewritten as:

$$I'_{out} = \frac{I_x I_y}{2I_B} \tag{3.189}$$

The absolute error is given by:

$$I_{error} = |I_{out} - I'_{out}| = 0 \tag{3.190}$$

This means the proposed circuit has very good performance with channel length mismatch.

As result, we can say that using the square-difference identity in the design of multiplying circuit reduces/cancels the errors resulting from the mismatch in carrier mobility parameter, transconductance parameter, threshold voltage, and channel length.

The proposed multiplier is compared with recently published works shown in Table (3.7). Comparing with references [20], [80], [86], the simulation results of the proposed circuit show a better performance in terms of supply voltage, input range, bandwidth, and silicon area. However, the advantages of the proposed circuit over the reference [81] are low power consumption, high relative error and small silicon area. Also comparing with reference [82], the proposed circuit has low supply voltage, wide input range and small silicon area. Finally, the proposed circuit is simulated using 0.18µm CMOS technology and it is used transistors with shorter channel-length (L=0.2µm) in comparison with previously published works shown in table (3.7) which used long channel-length transistors to reduce/cancel the error caused by carrier mobility reduction and channel length modulation, and hence improve the accuracy of the designed circuits.

Table 3.7 Comparison between the proposed multiplying and previously reported works

Ref.	Public. Year	Type (In/Out)	Tech. (µm)	Minim. L (µm)	Supply Voltage (V)	Input Range (µA)	Power Cons. (µW)	Relative Error (%)	-3 dB Frequency (MHz)	Area (μm^2)
[20]	2009	CI/CO	0.35	-	3.3	±10	240	1.15	44.9	-
[80]	2009	CI/CO	0.35	-	3.3	±10	340	1.1	41.8	-
[81]	2010	CI/CO	0.35	0.7	1.5	±20	1010	6.4	343	18603
[82]	2012	CI/CO	0.25	-	2.5	±10	168	-	278	331.5
[86]	2009	CI/CO	0.35	0.7	3.0	10	-	-	44	10000
This Work	**2013**	**CI/CO**	**0.18**	**0.2**	**1.5**	**±20**	**700**	**1.8**	**230**	**147**

CHAPTER 4

CONCLUSION AND FUTURE WORK

4.1 Conclusions

In this thesis, a new approach to compensate for the error resulting from carrier mobility reduction in circuits designed using short-channel MOSFET is developed. The approach is used in redesigning computational circuits based on MTL approach. This includes Square-rooting circuit, squaring circuit and multiplying circuit. The proposed circuits are designed using short channel MOSFETS in 0.18µm CMOS technology. The simulation results of the proposed square-rooting circuit have a better performance than prior art in terms of input range, bandwidth and silicon area. However, the major advantages of the proposed squaring circuit over previous circuits in terms of relative error, bandwidth and small silicon area. Comparing with most previous works, the proposed multiplier circuit has a better performance in terms of supply voltage, input range, bandwidth, and silicon area. Using the proposed blocks will enhance the accuracy of analog signal processing applications designed using short channel MOSFETS.

4.2 Directions for Future Work

There are some points to be looked at in the future;

- Layout and post layout simulation for the proposed circuits

- Considering errors due to other short-channel effect.
- Applying the technique for circuits design approaches other than MTL approach.

Appendix A

The process parameters used for this work, TSMC 0.18μm Technology:

```
.MODEL nenh NMOS (LEVEL   = 49
+VERSION = 3.1          TNOM    = 27              TOX     = 4.1E-9
+XJ      = 1E-7                 NCH     = 2.3549E17       VTH0    = 0.3694303
+K1      = 0.5789116    K2      = 1.110723E-3     K3      = 1E-3
+K3B     = 0.0297124    W0      = 1E-7                    NLX     = 2.037748E-7
+DVT0W   = 0            DVT1W   = 0               DVT2W   = 0
+DVT0    = 1.2953626    DVT1    = 0.3421545       DVT2    = 0.0395588
+U0      = 293.1687573   UA      = -1.21942E-9     UB      = 2.325738E-18
+UC      = 7.061289E-11  VSAT    = 1.676164E5      A0      = 2
+AGS     = 0.4764546     B0      = 1.617101E-7     B1      = 5E-6
+KETA    = -0.0138552            A1      = 1.09168E-3      A2      = 0.3303025
+RDSW    = 105.6133217           PRWG    = 0.5             PRWB    = -0.2
+WR      = 1                     WINT    = 2.885735E-9     LINT    = 1.715622E-8
+XL      = 0                     XW = -1E-8                DWG= 2.754317E-9
+DWB     = -3.690793E-9          VOFF    = -0.0948017      NFACTOR = 2.1860065
+CIT     = 0                     CDSC    = 2.4E-4          CDSCD   = 0
+CDSCB   = 0             ETA0    = 2.665034E-3     ETAB    = 6.028975E-5
+DSUB    = 0.0442223     PCLM    = 1.746064        PDIBLC1 = 0.3258185
+PDIBLC2 = 2.701992E-3   PDIBLCB = -0.1            DROUT   = 0.9787232
+PSCBE1  = 4.494778E10   PSCBE2  = 3.672074E-8           PVAG    = 0.0122755
+DELTA   = 0.01          RSH     = 7               MOBMOD  = 1
+PRT     = 0                     UTE     = -1.5            KT1     = -0.11
+KT1L    = 0                     KT2     = 0.022           UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11        AT      = 3.3E4
+WL      = 0                     WLN     = 1               WW      = 0
+WWN     = 1             WWL     = 0               LL      = 0
+LLN     = 1                     LW      = 0               LWN     = 1
+LWL     = 0                     CAPMOD  = 2               XPART   = 0.5
+CGDO    = 8.58E-10      CGSO    = 8.58E-10        CGBO    = 1E-12
+CJ      = 9.471097E-4   PB      = 0.8             MJ      = 0.3726161
+CJSW    = 1.905901E-10          PBSW    = 0.8             MJSW    = 0.1369758
+CJSWG   = 3.3E-10       PBSWG   = 0.8             MJSWG   = 0.1369758
+CF      = 0                     PVTH0   = -5.105777E-3            PRDSW   = -1.1011726
+PK2     = 2.247806E-3   WKETA   = -5.071892E-3            LKETA   = 5.324922E-4
+PU0     = -4.0206081    PUA     = -4.48232E-11    PUB     = 5.018589E-24
+PVSAT   = 2E3           PETA0   = 1E-4            PKETA   = -2.090695E-3    )
.MODEL penh PMOS (                      LEVEL   = 49
+VERSION = 3.1           TNOM    = 27              TOX     = 4.1E-9
```

+XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.3823437
+K1 = 0.5722049 K2 = 0.0219717 K3 = 0.1576753
+K3B = 4.2763642 W0 = 1E-6 NLX = 1.104212E-7
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 0.6234839 DVT1 = 0.2479255 DVT2 = 0.1
+U0 = 109.4682454 UA = 1.31646E-9 UB = 1E-21
+UC = -1E-10 VSAT = 1.054892E5 A0 = 1.5796859
+AGS = 0.3115024 B0 = 4.729297E-7 B1 = 1.446715E-6
+KETA = 0.0298609 A1 = 0.3886886 A2 = 0.4010376
+RDSW = 199.1594405 PRWG = 0.5 PRWB = -0.4947034
+WR = 1 WINT = 0 LINT = 2.93948E-8
+XL = 0 XW = -1E-8 DWG = -1.998034E-8
+DWB = -2.481453E-9 VOFF = -0.0935653 NFACTOR = 2
+CIT = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 3.515392E-4 ETAB = -4.804338E-4
+DSUB = 1.215087E-5 PCLM = 0.96422 PDIBLC1 = 3.026627E-3
+PDIBLC2 = -1E-5 PDIBLCB = -1E-3 DROUT = 1.117016E-4
+PSCBE1 = 7.999986E10 PSCBE2 = 8.271897E-10 PVAG = 0.0190118
+DELTA = 0.01 RSH = 8.1 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -0.11
+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9
+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4
+WL = 0 WLN = 1 WW = 0
+WWN = 1 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 7.82E-10 CGSO = 7.82E-10 CGBO = 1E-12
+CJ = 1.214428E-3 PB = 0.8461606 MJ = 0.4192076
+CJSW = 2.165642E-10 PBSW = 0.8 MJSW = 0.3202874
+CJSWG = 4.22E-10 PBSWG = 0.8 MJSWG = 0.3202874
+CF = 0 PVTH0 = 5.167913E-4 PRDSW = 9.5068821
+PK2 = 1.095907E-3 WKETA = 0.0133232 LKETA = -3.648003E-3
+PU0 = -1.0674346 PUA = -4.30826E-11 PUB = 1E-21
+PVSAT = 50 PETA0 = 1E-4 PKETA = -1.822724E-3)

Appendix B

Monte Carlo simulation statements (T-Spice) for threshold voltage and channel length variations are used for this work.

- **(Square-rooting Circuit)**

*****General*****

.lib "rf018.l " TT

.op

.probe

.option probev

.option probei

.option monteinfo=2

***** Parameters *****

.param L = 0.35u

.param LO = 0.35u

.param M = 2.5u

.param MU = 5u

.param O = 1u

.param W = 5u

.param WL = 2.5u

.param dvthp1=MC_dvthp1

.param MC_dvthp1=agauss(0,'0.41e-9/sqrt(M*L)',3) {*Gaussian distribution for threshold variation*}

.param dvthp4=MC_dvthp4

.param MC_dvthp4=agauss(0,'0.41e-9/sqrt(MU*L)',3) {*Gaussian distribution for threshold variation*}

.param Lt=MC_Lp

.param MC_Lp=gauss(0.35u,0.02,3) {*Gaussian distribution for channel length variation*}

*****Circuit*****

M1 5 shift1 Vdd Vdd pch W=M L=L {*I changed 9 to shift1when threshold voltage variation is used*}

M1 5 9 Vdd Vdd pch W=M L=Lt {*If channel length variation is used*}

M2 Gnd 5 9 9 pch W=M L=L

M3 7 7 Vdd Vdd pch W=MU L=L

M4 4 shift4 7 7 pch W=MU L=L {*I changed 5 to shift1when threshold voltage variation is used*}

M4 4 5 7 7 pch W=MU L=Lt {*If channel length variation is used*}

M5 9 10 Vdd Vdd pch W=W L=L

M6 10 10 Vdd Vdd pch W=W L=L

M7 8 10 Vdd Vdd pch W=W L=L

M8 5 1 Gnd Gnd nch W=W L=L

M9 1 1 Gnd Gnd nch W=W L=L

M10 4 1 Gnd Gnd nch W=W L=L

M11 4 8 Gnd Gnd nch W=W L=L

M12 8 8 Gnd Gnd nch W=W L=L

M13 6 1 Gnd Gnd nch W=WL L=L
M14 6 8 Gnd Gnd nch W=WL L=L
M15 6 7 Vdd Vdd pch W=MU L=L
M16 3 3 Gnd Gnd nch W=O L=LO
M17 6 6 3 3 nch W=O L=LO
M18 2 3 Gnd Gnd nch W=O L=LO
M19 11 6 2 2 nch W=O L=LO
RR_L Vdd N_11 R=10k
VVdd Vdd Gnd DC 2
IIx Vdd 1 DC Ix
IIy 10 Gnd DC 3u
vmc1 9 shift1 dvthp1 {*9 is a number which is changed to shift1*}
vmc4 5 shift4 dvthp4 {{*5 is a number which is changed to shift4*}
*****Analysis*****
.dc lin Ix 0 80uA 0.1uA sweep monte=100
.measure dc Ix max id(MM19)
.print dc id(MM19)
.end

➢ (Proposed Squaring Circuit)

*****General*****
.lib "rf018.l " TT
.op
.probe
.option probev
.option probei
.option monteinfo=2
*****Parameters*****
.param Ix = 0u
.param L = 0.2u
.param LO = 0.485u
.param M = 5u
.param MU = 2.5u
.param WO = 0.3u
.param dvthp1=MC_dvthp1
.param MC_dvthp1=agauss(0,'0.41e-9/sqrt(M*L)',3) {*Gaussian distribution for threshold variation*}
.param dvthp4=MC_dvthp4
.param MC_dvthp4=agauss(0,'0.41e-9/sqrt(MU*L)',3) {*Gaussian distribution for threshold variation*}
.param Lt=MC_Lp
.param MC_Lp=gauss(0.2u,0.02,3) {*Gaussian distribution for channel length variation*}
*****Circuit*****
M1 2 shift1 Vdd Vdd pch W=M L=L {*I changed 2 to shift1when threshold voltage variation is used*}
M1 2 2 Vdd Vdd pch W=M L=L {*If channel length variation is used*}
M2 3 3 2 2 pch W=M L=L

M3 6 6 Vdd Vdd pch W=MU L=L
M4 4 shift4 6 6 pch W=MU L=L {*I changed 3 to shift4when threshold voltage variation is used*}
M4 4 3 6 6 pch W=MU L=L {*If channel length variation is used*}
M5 4 6 Vdd Vdd pch W=MU L=L
M6 5 6 Vdd Vdd pch W=MU L=L
M7 1 1 Gnd Gnd nch W=M L=L
M8 3 1 Gnd Gnd nch W=M L=L
M9 4 1 Gnd Gnd nch W=M L=L
M10 5 1 Gnd Gnd nch W=MU L=L
M11 5 8 Gnd Gnd nch W=MU L=L
M12 8 8 Gnd Gnd nch W=M L=L
M13 6 8 Gnd Gnd nch W=M L=L
M14 5 5 Gnd Gnd nch W=WO L=LO
M15 11 5 Gnd Gnd nch W=WO L=LO
M16 8 8 9 9 pch W=M L=L
M17 9 9 10 10 pch W=M L=L
M19 10 10 Vdd Vdd pch W=M L=L
M18 8 9 7 7 pch W=M L=L
M20 7 10 Vdd Vdd pch W=M L=L
RR_L Vdd 11 R=10k
VVDD Vdd Gnd DC 1.5
IIb Vdd 1 DC 60u
IIx 9 Gnd DC Ix
vmc1 2 shift1 dvthp1 {*2 is a number which is changed to shift1*}
vmc4 3 shift4 dvthp4 {*3 is a number which is changed to shift4*}
*****Analysis *****
.dc lin Ix -40u 40u 0.1u sweep monte=100
.measure dc Ix max id(MM15)
.print dc id(MM15)
.end

Appendix C

Publications

Patents/ Disclosures:

[1] Munir Al-Absi and **Ibrahim Ass-saban**, " A new CMOS current mode squaring circuit with compensation for error due to carrier mobility reduction" filed with the U.S. Patent and Trademark Office (USPTO) on **November 5, 2013**, **Docket # 35000.34**

Refereed Journal /Magazine Articles:

[1] Munir A. AL-Absi and **Ibrahim As-sabban** "A New Highly Accurate CMOS Current-Mode Four Quadrant Multiplier", Arabian Journal for science and technology, published online, Dec 2014.

[2] Munir A. AL-Absi and **Ibrahim As-sabban** "A CMOS Current-mode Squaring Circuit free from Error Resulting from Carrier Mobility Reduction" Analog integrated circuit and signal processing" October 2014, Volume 81, Issue 1, pp 23-28.

Refereed Conference Publications:

[1] Munir Al-Absi and **Ibrahim As-sabban**, "A New Current-mode Squaring Circuit with Compensation for Error Resulting from Carrier Mobility Reduction," ELECO 2013 8th International Conference on Electrical and Electronics Engineering, Nov 2013.

[2] Munir Al-Absi and **Ibrahim As-sabban**, "Anew Square-Root Circuit Using Short Channel MOSFETs with Compensation for Error Resulting from Carrier Mobility Reduction," Electronics and Optoelectronics Vol. 1, No. 1, March 2013, pp.6-8.

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